iC-HC
ULTRA FAST DUAL HV-KOMPARATOR

preliminary

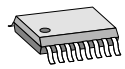
FEATURES

- Independent input supply voltage range up to 36 V
- Input voltage range down to VN
- Differential input voltage of 36 V max.
- Separate digital supply
- Programmable hysteresis resp. hold function
- Propagation delay typ. 5 ns
- Power save mode with propagation delay of typ. 20 ns
- Low current consumption stand-by mode
- TTL and CMOS compatible logic inputs and outputs
- 8 mA CMOS outputs
- Digital supply 3 to 5.5 V
- All pins protected against ESD

APPLICATIONS

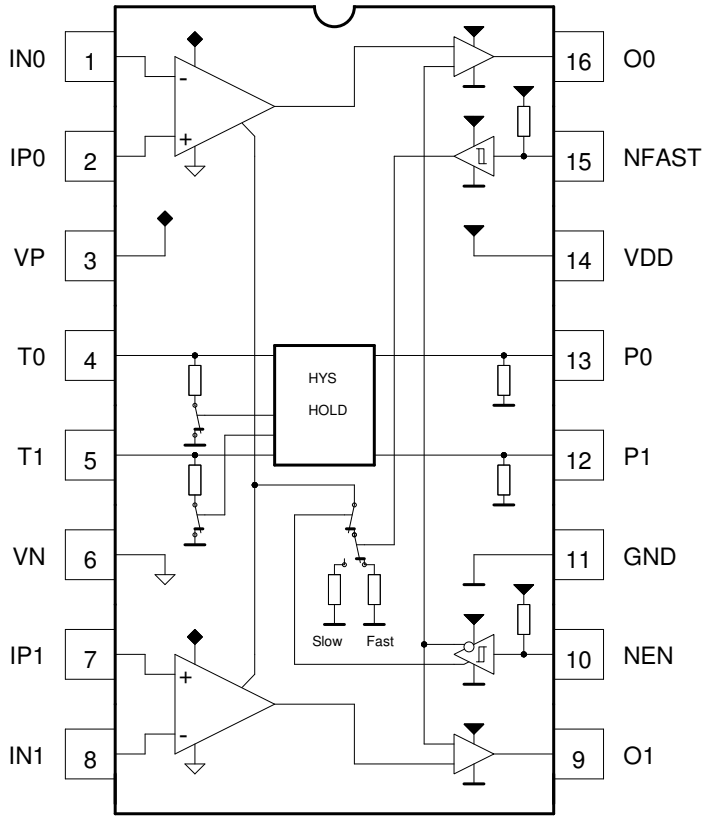
- Receiver for 24 V control systems
- A/D and D/A converters
- Signal conditioning
- Zero-crossing detectors
- I/Os, level shift
- Timing critical measurement equipment
- Time-to-digital converter interfaces (TDC)

PACKAGES



TSSOP16

BLOCK DIAGRAM



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DESCRIPTION

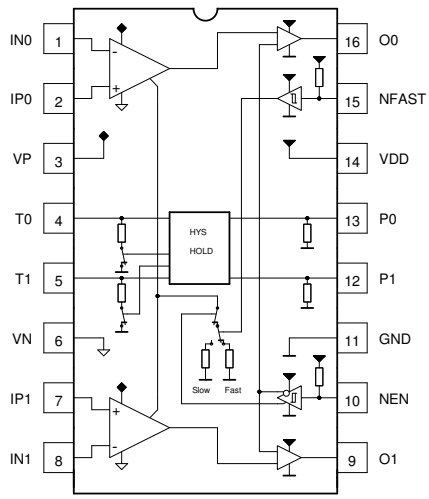
iC-HC features separate supply voltages for both the analogue inputs and the logic outputs. The logic power supply though must stay inside the boundaries of the inputs power supply.

The iC also features a zero current consumption standby mode as well as a current saving mode, the latter reducing the current consumption by 80%, though tripling the propagation delay.

Four values of input hysteresis (17 to 100 mV) or alternatively a hold function can be configured. The hold function blocks the toggling of the output for the configured hold time. For hold times > 100 µs external R/C networks can be used. Both hysteresis and hold function can be deactivated.

PACKAGING INFORMATION TSSOP16 to JEDEC

PIN CONFIGURATION TSSOP16



PIN FUNCTIONS

No.	Name	Function
1	IN0	Neg. Input Comparator 0
2	IP0	Pos. Input Comparator 0
3	VP	Pos. Power Supply
4	T0	Configuration Input / ext. RC
5	T1	Configuration input / ext. RC
6	VN	Neg. Power Supply
7	IP1	Pos. Input Comparator 1
8	IN1	Neg. Input Comparator 1
9	O1	Output Comparator 1
10	NEN	Standby (NEN = hi)
11	GND	Logic Ground
12	P1	Configuration Input
13	P0	Configuration Input
14	VDD	Logic Power Supply 5/3.3 V
15	NFAST	Power Save (NFAST = hi)
16	O0	Output Comparator 0

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VP	Pos. Supply Voltage		-0.5	46	V
G002	I(VP)	Current in VP		-5	5	mA
G003	V()	V(IPx), V(INx)		VN − 0.5	VP + 0.5	V
G004	I()	I(IPx), I(INx)		-2	+2	mA
G005	VDD	Voltage at VDD	referenced to VN	-0.5	46	V
G006	VDD	Logic Supply VDD	referenced to GND	-0.5	6	V
G007	I(VDD)	Current in VDD	referenced to GND	-5	20	mA
G008	I(VDD)	Current in VDD	referenced to VN	-5	5	mA
G009	GND	Voltage at GND	referenced to VN	-0.5	46	V
G010	I(GND)	Current in GND	referenced to VN	-5	5	mA
G011	V()	Voltage at output O0 and O1	referenced to GND	-0.5	6	V
G012	I()	Current in output O0 and O1	referenced to GND	-20	+20	mA
G013	I()	Current in iutput O0 and O1	referenced to VN	-5	+5	mA
G014	V()	V(NFAST,NEN,T0,T1,P0,P1)	referenced to GND	-0.5	6	V
G015	I()	I(NFAST,NEN,T0,T1,P0,P1)		-5	+5	mA
G016	Vd()	Susceptibility to ESD at all pins	HBM, 100 pF discharged through 1.5 kΩ		3	kV
G017	Ts	Storage Temperature Range		-40	150	°C
G018	Tj	Chip Temperature		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip/Ambient				140	K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDIFF	Differential Supply Voltage	VP − VN, VDD ≤ VP − 4 V	7		36	V
002	VP	Pos. Supply Voltage	VN = GND, VDD ≤ VP − 4 V	7		36	V
003	VN	Neg. Supply Voltage	VP = 9 V, VDD = 5 V	-27		0	V
004	I(VP)a	VP Current Consumption, active	NEN = lo; NFAST = lo NFAST = hi		 7.4 0.8	 12 1.5	 mA mA
005	I(VP)p	VP Current Consumption, passive	NEN = open (hi), NFAST = open (hi)		0	10	µA
006	I(VN)a	VN Current Consumption, active	NEN = lo; NFAST = lo NFAST = hi	 -8.5 -1	 -5.5 -0.55		 mA mA
007	I(VN)p	VN Current Consumption, passive	NEN = open (hi)	-10	0		µA
008	VDD	Logic Supply	VDD = VP − 4 V	3		5.5	V
009	I(VDD)p	VDD Current Consumption, passive	NEN open (hi), NFAST open (hi)		0	10	µA
010	I(VDD)a	VDD Current Consumption, active	V(NEN) = lo		0.78	2.3	mA
Outputs O0, O1							
101	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(), I() = -3.2 mA		0.1	0.2	V
102	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(), I() = -8 mA; VDD = 3 V VDD = 4.5 V		 0.25 0.2	 0.5 0.4	 V V
103	Vs()lo	Saturation Voltage lo	I() = 3.2 mA		0.12	0.25	V
104	Vs()lo	Saturation Voltage lo	I() = 8 mA; VDD = 3 V VDD = 4.5 V		 0.35 0.3	 0.7 0.6	 V V
Logic Inputs NFAST, NEN							
201	Vt()hi	Threshold Voltage hi	VDD = 5.5 V VDD = 3 V			2.4 1.7	V V
202	Vt()lo	Threshold Voltage lo	VDD = 5.5 V VDD = 3 V	1.4 0.8			V V
203	Vhys()	Input Hysteresis		10	90	250	mV
204	Rpu()	Pull-Up Resistor at NFAST, NEN referenced to VDD		35	50	70	kΩ
205	Rpd()	Pull-Down Resistor at T0, T1, P0, P1 referenced to GND		35	50	70	kΩ
Comparator Inputs INx, IPx							
301	Vcm()fast	Input Voltage Range	NFAST = lo	VN − 0.1		VP − 5	V
302	Vcm()	Input Voltage Range	NFAST = hi	VN − 0.1		VP − 4	V
303	ΔVi()	Permissible Differential Input Voltage	V(IPx) − V(INx)	-VDIFF		VDIFF	V
304	I()	Input Current at INx, IPx	I() = I(INx) + I(IPx); NFAST = lo NFAST = hi		 50 1	 150 4	 µA µA
305	Vos	Offset VOltage	P0 = lo (no hysteresis)	-30	0	30	mV
306	Vhys0	Input Hysteresis symmetrical	P1 = P0 = T1 = T0 = lo		34		mV
307	Vhys1	Input Hysteresis symmetrical	P1 = lo, P0 = hi, T1 = lo, T0 = hi		66		mV
308	Vhys2	Input Hysteresis symmetrical	P1 = lo, P0 = T1 = hi, T0 = lo		110		mV
309	Vhys3	Input Hysteresis symmetrical	P1 = lo, P0 = hi, T1 = T0 = hi		200		mV
310	tHoldint0	internal hold time	P1 = P0 = lo, T1 = lo, T0 = hi	0.6	1	1.6	µs
311	tHoldint1	internal hold time	P1 = P0 = lo, T1 = hi, T0 = lo	6	10	16	µs

ELECTRICAL CHARACTERISTICS

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
312	tHoldint2	internal hold time	P1 = P0 = lo, T1 = T0 = hi	60	100	160	µs
313	tHold	external hold time	P1 = P0 = hi, T0 (T1): ext. RC network with R referenced to VDD and C referenced to GND or VDD	0.7 * RC	RC	1.2 * RC	ms
Dynamic Parameters							
401	tp	Propagation Delay Ix → Ox	|ΔVi()| > 200 mV + Vhys in 0.5 ns, NFAST = lo; VDD = 5 V VDD = 3 V NFAST = hi		 9 11 20	 20 20 50	 ns ns ns
402	Δtp	Propagation Delay Difference	tp(Ox lo → hi) − tp(Ox hi → lo), symmetrical input signal; NFAST = lo NFAST = hi	 -25 -70		 25 70	 % %
403	trf()	Rise and Fall Time at O0, O1	Cl = 10 pF, Rl = 10 kΩ, VDD = 5 V, 10 % ↔ 90 %		1	2	ns
404	tpmin	Minimum Pulse Duration	NFAST = lo, VDD = 5 V NFAST = lo, VDD = 3 V NFAST = hi, VDD = 3 V		9 11 20	20 25 50	ns ns ns
Hold-Timer T0, T1							
501	Rext	ext. resistor	P0 = P1 = hi, hold time = R * C, Rext referenced to VDD	2			kΩ
502	Cext	ext. capacitor	P0 = P1 = hi, holdtime = R * C, Cext referenced to GND or VDD	0			pF

DESCRIPTION OF FUNCTION

For noise suppression four symmetrical hysteresis settings can be configured as per Table 4.

P1	P0	T1	T0	Hys./Hold
0	0	0	0	no Hys./Hold
0	0	0	1	1 µs Hold
0	0	1	0	10 µs Hold
0	0	1	1	100 µs Hold
0	1	0	0	±17 mV Hys.
0	1	0	1	±33 mV Hys.
0	1	1	0	±55 mV Hys.
0	1	1	1	±100 mV Hys.
1	0	X	X	no Hys./Hold
1	1	R/C*	R/C*	Hold with ext. R/C

Table 4: Configuration

Alternatively a hold function can be used for noise suppression: Following each falling or rising edge at the outputs the toggling is blocked for the configured hold time. With the hold time elapsed the output will follow the input signal instantly. Table 4 shows three pre-set hold times. The hold function has the advantage over the hysteresis, that it does not shift the input switching threshold. With the aid of the hold function even extreme interferences like e.g. "bouncing" can be completely blanked. Figure 3 shows a respective example of a zero-crossing detector.

Three hold times are pre-configured and can be chosen according to Table 4 without external circuitry. For different hold times external R/C networks can be used at T0 and T1 (P0 and P1 = hi)). Both hold timers work independently, so individual hold times can be chosen.

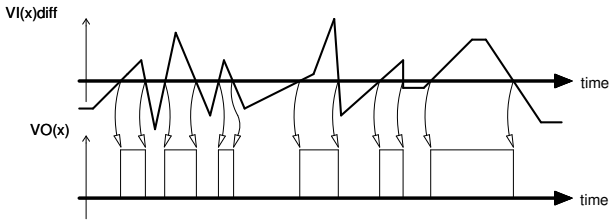


Figure 1: Switching characteristic without Hysteresis/Hold

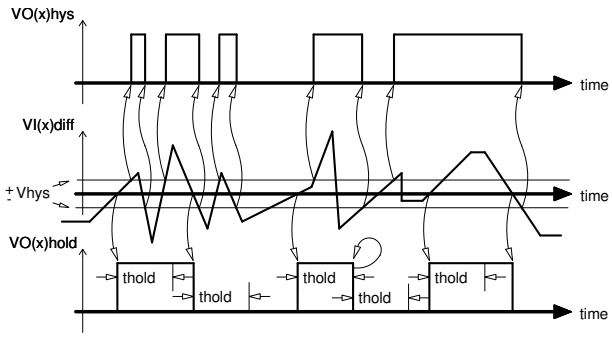


Figure 2: Switching characteristic with hysteresis resp. hold function

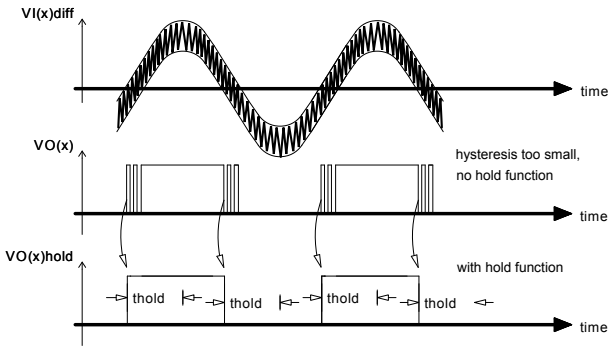


Figure 3: Blanking of noise using the hold function

* external R/C network

Hold function with external R/C network

Using external R/C networks at TO and T1 results in signals as shown in Figure 5. The threshold is set to 2/3 VDD, hence the hold time is calculated using τ to t_{hold} = Rext * Cext. The discharging is accomplished via ca. 25 Ω and hence neglible, since the ext. resistor (vs. VDD) may not be smaller than 2 kΩ. The hold time for comparator 0 is set by R0 and C0, whereas R1 and C1 set the hold time for comparator 1.

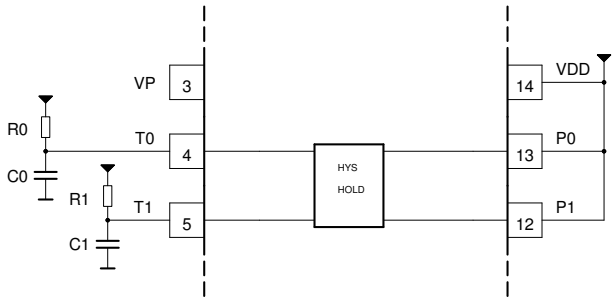


Figure 4: R/C network connection

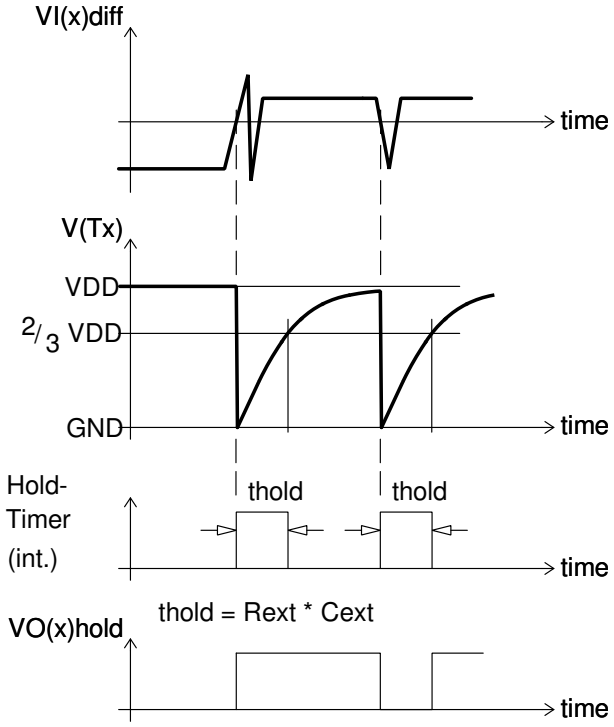


Figure 5: Signals at T0 (T1) with ext. R/C network

EVALUATION BOARD

For the iC-HC an Evaluation Board is available for test purposes. The following figures show the schematic diagram and the component side of the test PCB.

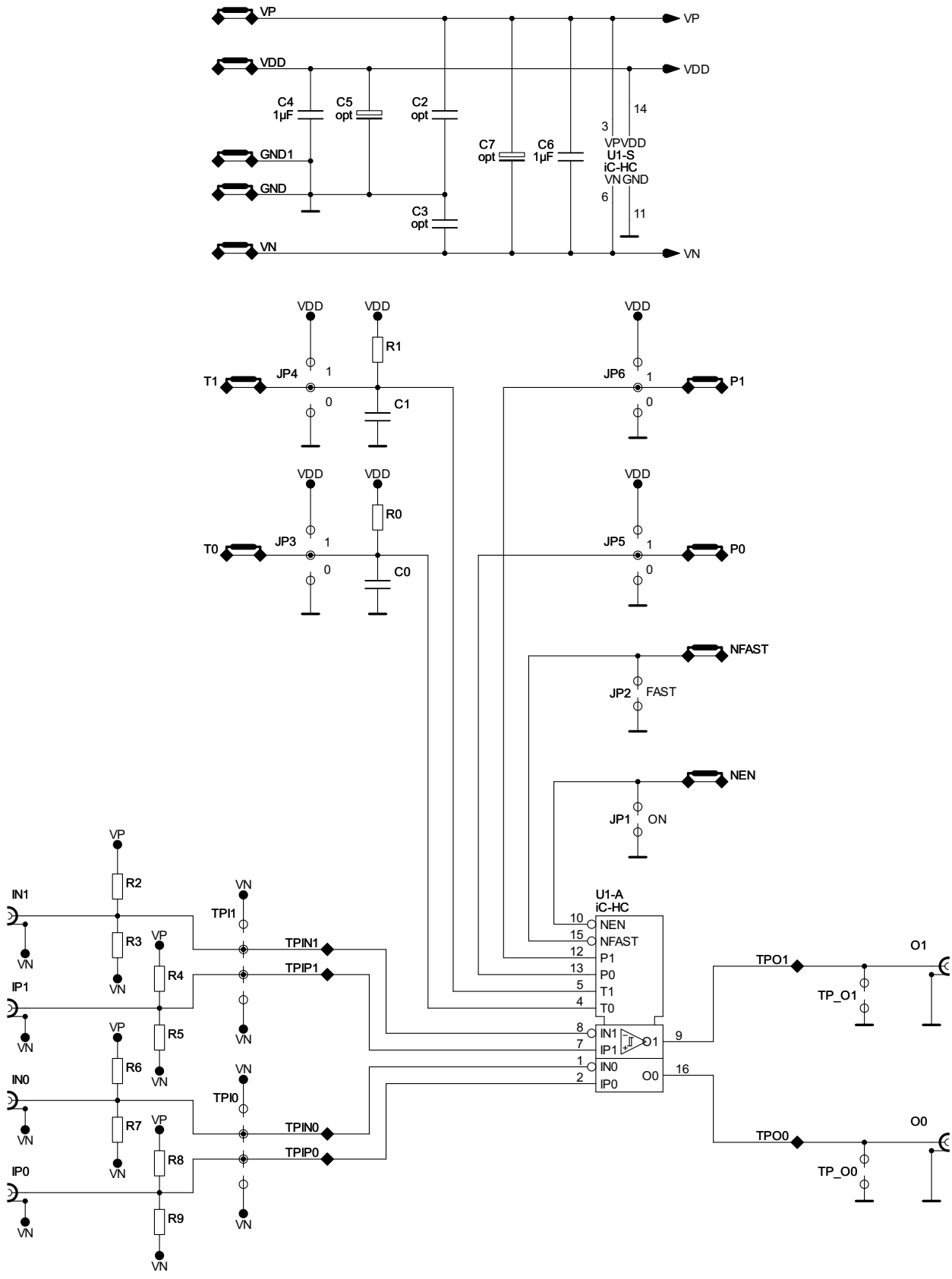


Figure 6: Schematic of the evaluation board

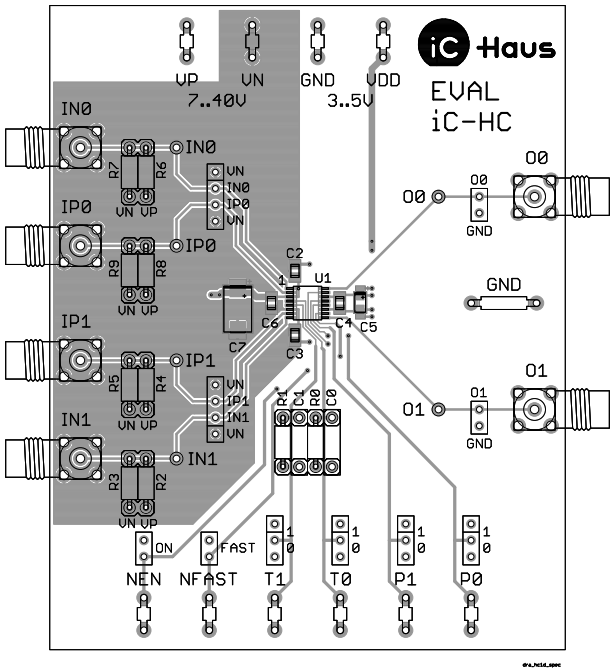


Figure 7: Evaluation board (component side)

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ORDERING INFORMATION

Type	Package	Order Designation
iC-HC	TSSOP16	iC-HC TSSOP16
iC-HC	Evaluation Board	iC-HC EVAL HC1D

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