iC-HO
General Purpose Sensor Interface

preliminary

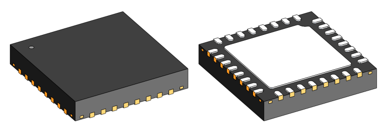
FEATURES

- 16-bit analog-to-digital conversion
- Integrated configurable linearization for sensor signal characteristic curve
- Configurable temperature drift compensation
- Analog PGA input, low noise, ultra low offset
- Sensor signal offset correction
- Configurable low noise ratiometric differential analog output
- Digital sensor data output
- Signal and system monitoring (heater breakdown, max. heater power, sensing element breakdown, sensor signal range check)
- Open-drain error output signalling
- Integrated 8 bit thermometer
- Triple controlled constant current sources
- SPI master for SPI EEPROM
- SPI communication and configuration interface
- Device setup from serial EEPROM and SPI
- 5 V supply

APPLICATIONS

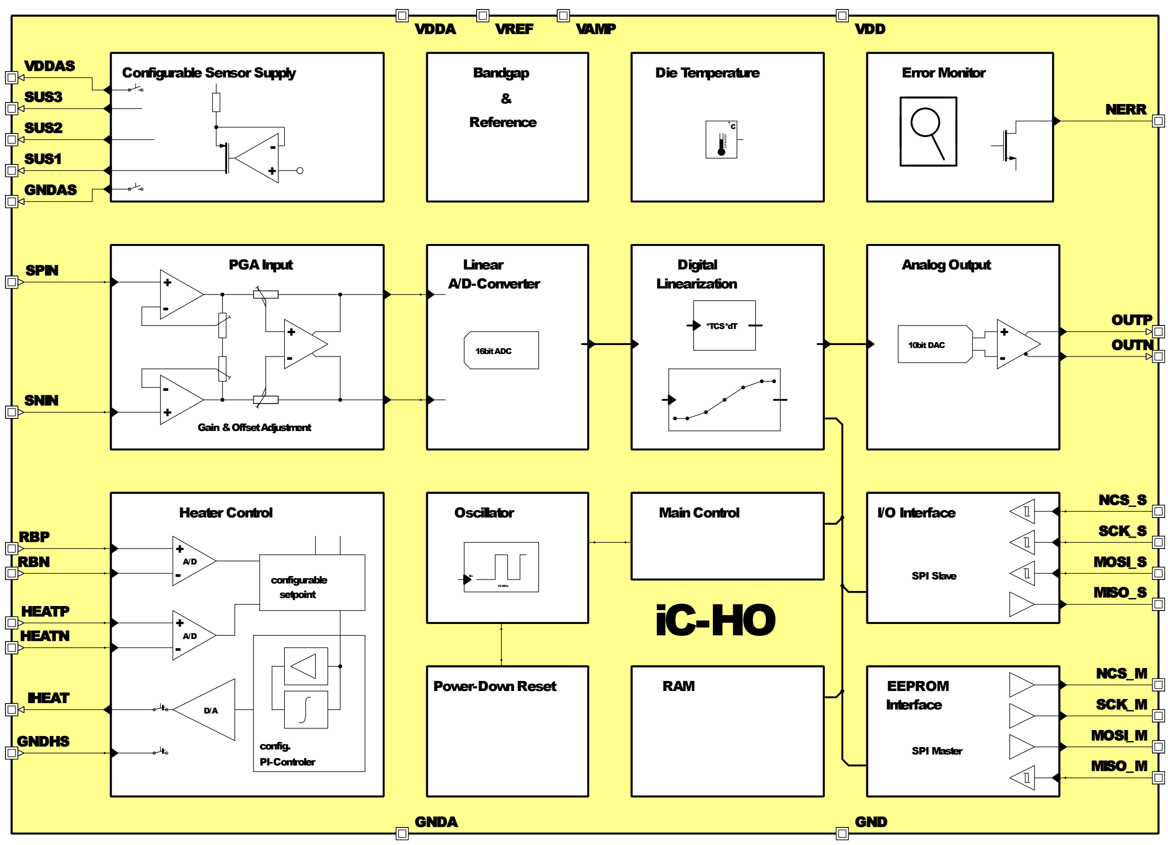
- Flow sensors
- Pressure sensors
- Gas sensors

PACKAGES



QFN32 5mm x 5mm

BLOCK DIAGRAM



DESCRIPTION

iC-HO is a monolithic general purpose sensor interface and supports different sensors, providing both digital and analog output of the conditioned sensor signals.

Typical applications are:
- flow sensors
- pressure sensors
- gas sensors

The sensor signal input stage is an instrumentation PGA architecture. Amplification can be programmed and offset can be calibrated. The calibration range for the offset depends on the selected source and it is possible to select a constant offset or ratiometric offset calibration. It is possible to bias three sensor resistors with a constant current, wherein two constant current sources have an excellent matching.

For temperature dependent offset values it is possible to track dynamically. The calibration reference temperature and the temperature coefficient can be set or the dynamical tracking turned off. The internal digital 8-bit temperature sensor is available and offset calibratable. The temperature compensations can use the integrated or an external temperature sensor.

iC-HO contains a fast sensor signal analog-to-digital converter with 16-bit resolution. Either the analog to digital converters output directly or already the difference between two conversions is applicable. For linearization a piece-wise linear interpolation of values stored in a look-up table (LUT) is used to calculate the gain and offset for a given analog-to-digital converter's output. Up to 10 breakpoints within the LUT are possible. Breakpoints can be placed across the analog-to-digital converter's output freely with an 8-bit addressing resolution.

The digitally implemented PI controller can either be operated in temperature offset or absolute temperature mode and control a sensor's heating unit. The 12-bit A/D converter ”bulk” converts the analog voltage drop over the bulk resistor between two pins and the 14-bit A/D converter ”Heater” converts the analog voltage drop over the heater resistor between two pins. Both are observable via SPI interface. The 12-bit D/A converter ”Heater” outputs a current and is, depending on the programmed controller mode, constantly settable or controlled by the PI controller. To protect the heater resistor the PI controllers output can be limited to a maximum value.

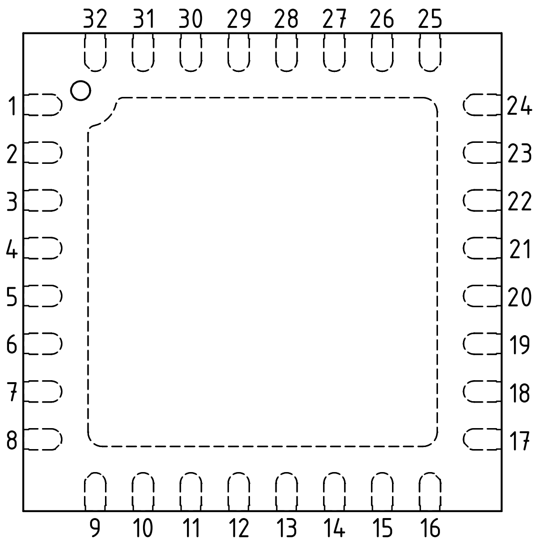
For operation with an external microcontroller iC-HO provides an SPI slave interface. The calibration sequence can also be operated through the external SPI slave microcontroller interface. The internal configuration can be stored automatically to an SPI EEPROM and the CRC checksum is updated and written to the EEPROM as well. iC-HO does also support a stand alone operation with the configuration from an external EEPROM. After power-on the configuration data is read automatically from the external SPI EEPROM. If the third attempt fails the reading procedure is stopped, reset values take place and an error is set.

A 10-bit digital to analog converter with ratiometric differential analog output at pins is implemented. The sensor data output as well as error messages, bulk temperature, heater temperature and on-chip temperature can also be read via SPI interface. It is also possible to disable some of these error bits by a configured mask. If an unmasked error occurs the respective error bit in the status register and the open drain output pin NERR is pulled down.

Internal reference voltages for the analog-to-digital converter's or external reference voltages can be used. For analog calibration internal analog signals and the internal bias current can be output.

PACKAGING INFORMATION

PIN CONFIGURATION QFN32 5 mm x 5 mm (topview)



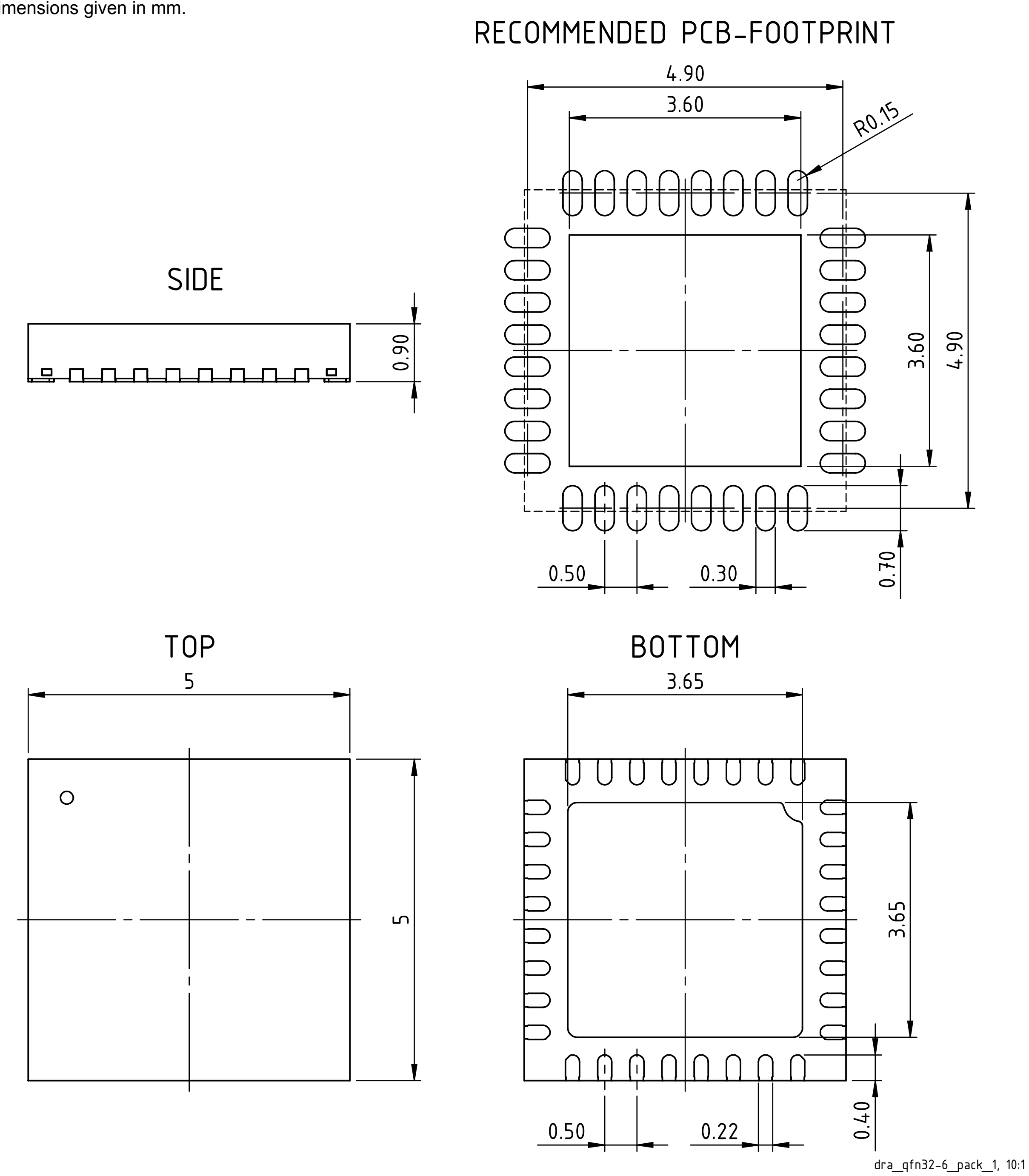
PIN FUNCTIONS

No.	Name	Function
1	VDDAS	Switched Sensor Supply Output Voltage
2	IHEAT	Heater DAC Current Output
3	SPIN	Sensor Positive Input
4	SNIN	Sensor Negative Input
5	GNDAS	Switched Sensor Ground
6	GNDHS	Switched Heater Ground
7	HEATN	Heater Resistor ADC Negative Port
8	HEATP	Heater Resistor ADC Positive Port
9	RBN	Bulk Resistor ADC Negative Port
10	n.c.	not connected
11	RBP	Bulk Resistor ADC Positive Port
12	n.c.	not connected
13	VDD	+4.5 to +5.5 V Digital Supply Voltage
14	GND	Digital Ground
15	NCS_M	SPI EEPROM(master), Not Chip Select
16	SCK_M	SPI EEPROM(master), Clock
17	MOSI_M	SPI EEPROM(master), Master Out Slave In
18	MISO_M	SPI EEPROM(master), Master In Slave Out
19	NCS_S	SPI I/O(slave), Not Chip Select
20	SCK_S	SPI I/O(slave), Clock
21	MOSI_S	SPI I/O(slave), Master Out Slave In
22	MISO_S	SPI I/O(slave), Master In Slave Out
23	NERR	Error Message Output
24	OUTP	Positive Analog Output
25	OUTN	Negative Analog Output
26	GNDA	Analog Ground
27	VDDA	+4.5 to 5.5 V Analog Supply Voltage
28	VAMP	Converter Reference Voltage
29	VREF	Converter Reference Voltage
30	SUS3	Sensor Biasing Output 3
31	SUS2	Sensor Biasing Output 2
32	SUS1	Sensor Biasing Output 1
TP	TP	Thermal Pad

The *Thermal Pad* is to be connected to a *Ground Plane* (GNDA) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC HO label and coding is subject to change).

PACKAGE DIMENSIONS

All dimensions given in mm.



ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at all pins	referenced to GNDA	-0.3	6	V
G002	I()	Current in VDD,VDDA		-100	20	mA
G003	I()	Current in VDDAS, GNDAS		-7.5	7.5	mA
G004	I(HEATP)	Current in IHEAT		-90	20	mA
G005	I(HEATN)	Current in GNDHS		-20	90	mA
G006	I(NERR)	Current in NERR		-20	60	mA
G007	I()	Current in MISO_S, NCS_M, SCK_M, MOSI_M		-60	60	mA
G008	I()	Current in all other pins		-20	20	mA
G009	Vd()	ESD susceptibility at all pins	HBM 100pF discharged through 1.5kΩ		2	kV
G010	Tj	Junction temperature		-40	150	°C
G011	Ts	Storage temperature range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-25		100	°C
T02	Rthja	Thermal Resistance Chip to Ambient	surface mounted to PCB according to JEDEC 51		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDA = 5 V ± 10%, GND = GNDA, Tj = -25...105 °C, IBN calibrated to 100 µA, reference point GNDA, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD,VDDA	Permissible Supply Voltage		4.5		5.5	V
002	I(VDDA)	Supply Current in VDDA	Tj = 27 °C, IDLE mode		9		mA
003	I(VDD)	Supply Current in VDD	Tj = 27 °C, IDLE mode		9		mA
004	Vc()hi	Clamp Voltage hi	Vc()hi = V() – VDD, I() = 1 mA Pins: NERR, MISO_S, MOSI_S, SCK_S, NCS_S, MISO_M, MOSI_M, SCK_M, NCS_M	0.4		1.5	V
005	Vc()hi	Clamp Voltage hi	Vc()hi = V() – VDDA, I() = 100 µA Pins: SPIN, SNIN, RBP, RBN, HEATP, HEATN	0.4		1.5	V
006	Vc()lo	Clamp Voltage lo	I() = -1 mA	-1.5		-0.3	V
Signal Conditioning and Inputs							
101	Iin()	Input Current at SPIN, SNIN			t.b.d.		pA
102	Vin()	Permissible Input Voltage at SPIN, SNIN		0.03		VDDA – 1.5	V
103	V()	Permissible Voltage at S1P, S1N		0.03		VDDA – 0.02	V
104	Av_{stage1}	Selectable PGA Amplification Stage 1	GAIN1 = 0x0 GAIN1 = 0x1 GAIN1 = 0x2 GAIN1 = 0x3		1.1 2 3 4		
105	Av_{stage2}	Selectable PGA Amplification Stage 2	GAIN2 = 0x0 GAIN2 = 0x1 GAIN2 = 0x2 GAIN2 = 0x3		1 3 5 12		
106	VOScal	Offset Calibration Range	referenced to input V(SPIN) – V(SNIN), REFOS = 0x1 GAIN1 = 0 GAIN1 = 1 GAIN1 = 2 GAIN1 = 3		 ±33.0 ±99.9 ±88.8 ±74.9		 mV mV mV mV
107	ΔVOSdiff	Differential Linearity Error of Offset Correction		-0.5		0.5	LSB
108	ΔVOSint	Integral Linearity Error of Offset Correction	referenced to maximum reading	-5		5	LSB
109	tcos	Temperature Coefficient Offset Correction Tracking	TCOS = 0x00 TCOS = 0xFF		-6012 1770		ppm/°C ppm/°C
110	fg()	Input PGA Cut-Off Frequency			t.b.d.		kHz
111	V_{os}	PGA Offset Voltage	V() = V(ADP) – V(ADN), V(SPIN) = V(SNIN)		t.b.d.		µV
Analog to Digital Conversion							
201	RES	A/D Converter Resolution		16			bit
202	tconv	Conversion Time	continuous mode switched supply mode		100 200		µs µs
204	DNL	Differential Nonlinearity		-1		1	LSB
205	Vana	Maximum Input Voltage	Vana = V(ADP) – V(ADN)	-2		2	V
Heater Control: RBP, RBN, HEATP, HEATN, IHEAT, GNDHS							
301	Iin()	Input Current at RBP, RBN, HEATP, HEATN			t.b.d.		pA
302	Vin()diff	Permissible Input Voltage Range A/D Converter Bulk Thermometer	V() = V(RBP) – V(RBN), minimum input voltage maximum input voltage		 0 1200		 mV mV
303	Vin()cm	Permissible Common Mode Input Voltage RBN, RBP		0.015		VDDA – 1.5	V
304	RES_{bulk}	Resolution A/D Converter Bulk Thermometer			12		bit

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDA = 5 V ± 10%, GND = GNDA, Tj = -25...105 °C, IBN calibrated to 100 µA, reference point GNDA, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
306	DNL_{bulk}	Differential Nonlinearity A/D Converter Bulk Thermometer		-1		1	LSB
307	V()diff	Permissible Input Voltage Range A/D Converter Heater	V() = V(HEATP) – V(HEATN) minimum input voltage maximum input voltage		 0 3300		 mV mV
308	Vin()cm	Permissible Common Mode Input Voltage HEATN, HEATP		0.015		VDDA – 1.5	V
309	RESh	Resolution A/D Converter Heater			14		bit
311	DNL_{heater}	Differential Nonlinearity A/D Converter Heater		-1		1	LSB
312	$tconv_{bulk}$	Conversion Time A/D Converter Bulk			100		µs
313	$tconv_{heater}$	Conversion Time A/D Converter Heater			100		µs
314	tcr	Resistor Temperature Coefficient	RTCR = 0x0, TCR = 0x00 RTCR = 0x0, TCR = 0xFF RTCR = 0x1, TCR = 0x00 RTCR = 0x1, TCR = 0xFF		1953 2926 2929 3902		ppm/°C ppm/°C ppm/°C ppm/°C
315	I()	Controller Output D/A-Converter Heater Current Range	I = I(IHEAT), IHEAT = 0x000 IHEAT = 0xFFF, RIHEAT = 0x0 IHEAT = 0xFFF, RIHEAT = 0x1		 0 -35.83 -71.66		 mA mA mA
316	RESo	Controller Output D/A Converter Heater Current Resolution			12		bit
317	INL_{IHEAT}	Integral Nonlinearity D/A Converter Heater Current	referenced to maximum reading	-8		8	LSB
318	DNL_{IHEAT}	Differential Nonlinearity D/A Converter Heater Current		-1		1	LSB
319	Vs()hi	Saturation Voltage hi	Vs()hi = V(VDDA) – V(IHEAT), I(IHEAT) = 0xFF, CMODE = 0x1			1	V
320	Kp	Proportional Gain PI Controller	CKP = 0x00 CKP = 0xFF		0 2040		
321	Ki	Integral Gain PI Controller	CKI = 0x00 CKI = 0xFF		0 255		
322	fs	Controller Sampling Frequency			9.766		kHz
323	$T1_{force}$	Set-Point Temperature 1	UB20, UH20 calibrated T1F = 0x00 T1F = 0x7F		 25 660		 °C °C
324	$T2_{force}$	Set-Point Temperature 2	UB20, UH20 calibrated T2F = 0x00 T2F = 0x7F		 25 660		 °C °C
325	$t(T1_{force})$	Period Temperature 1	T1T = 0x00 T1T = 0xFF		0.1 25.6		s s
326	$t(T2_{force})$	Period Temperature 2	T2T = 0x00 T2T = 0xFF		0.1 25.6		s s
327	$R(GNDHS)_{on}$	Switch on Resistance GNDHS				10	Ω
328	$R(GNDHS)_{off}$	Switch off Resistance GNDHS		1			MΩ
329	$R(IHEAT)_{off}$	off resistance IHEAT		1			MΩ
Sensor Biasing: SUS1, SUS2, SUS3, VDDAS, GNDAS							
401	Ibu	Bias Current Bulk Thermometer	I(SUS3), IBULK = 0x0 IBULK = 0x1 IBULK = 0x2 IBULK = 0x3		 -140 -280 -420 -560		 µA µA µA µA
402	Ise1	Bias Current Sensor 1	I(SUS1)		-560		µA
403	Ise2	Bias Current Sensor 2	I(SUS2)		-560		µA
404	Rcerr	Sensor Current Ratio Error	Rcerr = Ise1 / Ise2 – 1	-10000		10000	ppm

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDA = 5 V ± 10%, GND = GNDA, Tj = -25...105 °C, IBN calibrated to 100 µA, reference point GNDA, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
405	Vs()hi	Saturation Voltage hi SUS1	Vs()hi = V(VDDA) – V(SUS1), I() = Ise1			1	V
406	Vs()hi	Saturation Voltage hi SUS2	Vs()hi = V(VDDA) – V(SUS2), I() = Ise2			1	V
407	Vs()hi	Saturation Voltage hi SUS3	Vs()hi = V(VDDA) – V(SUS3), I() = Ibu, IBULK = 0x3			1	V
408	$R()_{on}$	Switch on Resistance VDDAS, GNDAS				100	Ω
409	$R()_{off}$	Switch off Resistance VDDAS, GNDAS		1			MΩ
Analog Output: OUTP, OUTN							
501	RESa	Analog Output Resolution			10		bit
502	INL	Integral Nonlinearity D/A Converter		-2		2	LSB
503	DNL	Differential Nonlinearity D/A Converter		-0.5		0.5	LSB
504	Vdiff()	Differential Output Range D/A Converter	Vdiff() = V(OUTP) – V(OUTN) minimum output voltage maximum output voltage		-80 80		% VDDA % VDDA
505	Vcm()	Analog Output Common Mode Voltage	Vcm() = VREF		50		% VDDA
506	ta	Analog Output Refresh Rate	continuous mode	1	0.1		ms
508	Isc()hi	Short-Circuit Current hi	V() = GNDA			-2	mA
509	Isc()lo	Short-Circuit Current lo	V() = VDDA	2			mA
Bias Current Source and Reference Voltages: VREF, VAMP							
A01	IBN	Bias Current Source	IBN calibrated to 100µA	92.5	100	107.5	%
A02	V(VREF)	Ratiometric Reference Voltage		41	43	45	% VDDA
A03	V(VAMP)	AD Reference Amplitude Voltage	V() =V(VREF) – V(VAMP)		1.24		V
A05	C(VREF)	Capacitance VREF	low ESR ceramic capacitor required		t.b.d.		nF
A06	C(VAMP)	Capacitance VAMP	low ESR ceramic capacitor required		t.b.d.		nF
8 bit Digital Temperature Monitoring							
B01	DTEMP	Digital Temperature Representation	Tj = -40 °C Tj = 20 °C Tj = 100 °C		0x16 0x52 0xA2		
B02	ΔT	Measurement Resolution			1		°C/LSB
B03	T_{os}	Measurement Offset Error	Tj = -40...125 °C	-7		7	°C
B04	INL	Integral Linearity Error	Tj = -40...125 °C	-3		3	LSB
B05	DNL	Differential Linearity Error	Tj = -40...125 °C	-1		1	LSB
B06	Tr	Refresh Rate	maximum change ± 1 LSB		2		µs
Clock Oscillator							
C01	fosc	Clock Frequency			10		MHz
Error Message Output: NERR							
E01	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
E02	Isc()lo	Short-Circuit Current lo		4		60	mA
E03	I()hi	Leakage Current hi			t.b.d.		nA
I/O Interface: NCS_S, SCK_S, MOSI_S, MISO_S							
M01	Vt()hi	Input Threshold Voltage hi at NCS_S, SCK_S, MOSI_S				2	V
M02	Vt()lo	Input Threshold Voltage lo at NCS_S, SCK_S, MOSI_S		0.8			V
M03	Vt()hys	Input Hysteresis at NCS_S, SCK_S, MOSI_S		150	250		mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDA = 5 V ± 10%, GND = GNDA, Tj = -25...105 °C, IBN calibrated to 100 µA, reference point GNDA, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
M04	Ipu()	Input Pull-Up Current at NCS_S	V(NCS_S) = 0 . . . VDD – 1 V	-65	-30	-5	µA
M05	Vpu()	Input Pull-Up Voltage at NCS_S	Vpu() = VDD – V(NCS_S), I() = -5 µA			650	mV
M06	Ipd()	Input Pull-Down Current at SCK_S and MOSI_S	V() = 1 V . . . VDD	5	30	75	µA
M07	Vpd()	Input Pull-Down Voltage at SCK_S and MOSI_S	I() = 5 µA			650	mV
M08	Vs()hi	Saturation Voltage high at MISO_S	Vs()hi = VDD – V(MISO_S), I(MISO_S) = -4 mA			500	mV
M09	Vs()lo	Saturation Voltage low at MISO_S	I(MISO_S) = 4 mA			600	mV
M10	Isc()hi	Short-Circuit Current hi at MISO_S		-60		-15	mA
M11	Isc()lo	Short-Circuit Current lo at MISO_S		15		60	mA
M12	f()	Permissible Clock Frequency at SCK_S				2	MHz
EEPROM Interface: NCS_M, SCK_M, MOSI_M, MISO_M							
N01	Vt()hi	Input Threshold Voltage hi at MISO_M				2	V
N02	Vt()lo	Input Threshold Voltage lo at MISO_M		0.8			V
N03	Vt()hys	Input Hysteresis at MISO_M		150	250		mV
N04	Ipd()	Input Pull-Down Current at MISO_M	V() = 1 V...VDD	5	30	75	µA
N05	Vpd()	Input Pull-Down Voltage at MISO_M	I() = 5 µA			650	mV
N06	Vs()hi	Saturation Voltage high at NCS_M, SCK_M, MOSI_M	Vs()hi = VDD – V(), I() = -4 mA			500	mV
N07	Vs()lo	Saturation Voltage low at NCS_M, SCK_M, MOSI_M	I() = 4 mA			600	mV
N08	Isc()hi	Short-Circuit Current hi at NCS_M, SCK_M, MOSI_M		-60		-15	mA
N09	Isc()lo	Short-Circuit Current lo NCS_M, SCK_M, MOSI_M		15		60	mA
N10	f()	Clock Frequency at SCK_M			1.25		MHz
Power-Down-Reset							
P01	VDDon	Turn-on Threshold VDD (power on release)	increasing voltage VDD	3.6	3.9	4.3	V
P02	VDDoff	Turn-off Threshold VDD (power-down reset)	decreasing voltage VDD	3.1	3.4	3.8	V
P03	VDDhys	Hysteresis	VDDhys = VDDon – VDDoff	400			mV

OPERATING REQUIREMENTS: I/O Interface (NCS_S, SCK_S, MOSI_S, MISO_S)

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI Slave Interface						
I001	t_{C1}	Permissible Cycle Time	see Elec. Char. No.: M12	1/f()		
I002	t_{W1}	Wait Time: between NCS lo → hi and NCS hi → lo		500		ns
I003	t_{S1}	Setup Time: NCS lo before SCK lo → hi		50		ns
I004	t_{P1}	Propagation Delay: MISO stable after NCS hi → lo			100	ns
I005	t_{P2}	Propagation Delay: MISO high impedance after NCS lo → hi			100	ns
I006	t_{H1}	Hold Time: NCS lo after SCK lo → hi	valid for SPI mode 3	400		ns
I007	t_{S2}	Setup Time: MOSI stable before SCK lo → hi		100		ns
I008	t_{H2}	Hold Time: MOSI stable after SCK lo → hi		100		ns
I009	t_{P3}	Propagation Delay: MISO stable after MOSI change	mode: repeating MOSI on MISO		100	ns
I010	t_{P4}	Propagation Delay: MISO stable after SCK hi → lo	mode: sending data on MISO		100	ns
I011	t_{W2}	Wait Time: SCK stable after NCS lo → hi		500		ns
I012	t_{H3}	Hold Time: NCS lo after SCK hi → lo	valid for SPI mode 0	400		ns
I013	t_{L1}	Clock Signal lo Level Duration		100		ns
I014	t_{L2}	Clock Signal hi Level Duration		100		ns

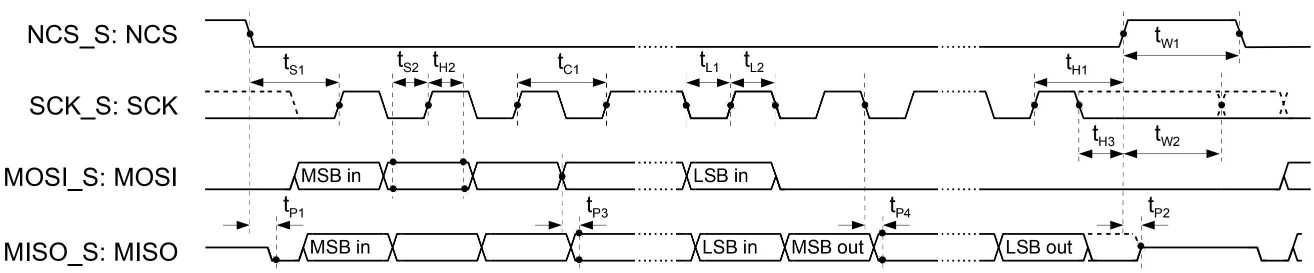


Figure 1: Timing SPI Slave Interface

CONFIGURATION PARAMETERS

Operating Mode
OPMODE: Operating Mode (P. 15)
CHM: Converter Mode (P. 16)

Status Register
DTEMP: Die Temperature (P. 29)
OSACT: Actual Offset Correction Value (P. 24)
IHEATACT: Actual Heater Current Value (P. 22)
TBACT: Actual Bulk Resistor Temperature (P. 21)
THACT: Actual Heater Resistor Temperature (P. 21)
DSENS: Sensor Data (P. 27)
ERROR: Error Notification (P. 28)

Self and Sensor Biasing
CFGIBN: Bias Trimming (P. 18)
IBULK: Bulk Resistor Biasing (P. 18)
ENREF: Enable AD Reference Buffers (P. 18)
ADOS: Disable IHEAT/SUS3 Current Source (P. 21)

PI Controller Configuration
CMODE: Controller Mode (P. 19)
RTCR: Temperature Coefficient Heater/Ambient Temperature Sensor Range (P. 21)
TCR: Temperature Coefficient Heater/Ambient Temperature Sensor (P. 21)
UB20: Bulk Temperature Resistor Reference Reading (P. 15)
UH20: Heater Reference Reading (P. 15)
CKP: Amplification Proportional Controller (P. 20)
CKI: Amplification Integral Controller (P. 20)
T1F: Temperature Set Point 1 (P. 20)
T2F: Temperature Set Point 2 (P. 20)
T1T: Period Set Point 1 (P. 20)
T2T: Period Set Point 2 (P. 20)
TSENSRD1: Sensor Read Time 1 (P. 20)
TSENSRD2: Sensor Read Time 2 (P. 20)
IHEAT: Controller Output Current (P. 22)
RIHEAT: Controller Output Current Range (P. 22)
CIMAX: Maximum Controller Output Current (P. 22)
SWACT: Activate alternating Heater and Sensor Switching (P. 20)
RAWAD: Debug: UH/UB/RAWAD to status register THACT/TBACT/DSENS (P. 19)

Sensor Signal Conditioning
GAIN1: Gain Factor Stage 1 (P. 23)
GAIN2: Gain Factor Stage 2 (P. 23)
REFOS: Offset Correction Reference (P. 23)
OS: Offset Correction (P. 23)
TCOS: Temperature Coefficient Sensor Offset (P. 24)

Digital Linearization
LUTA1 . . . LUTA8: LUT Address Breakpoints (P. 26)
LUTD0 . . . LUTD9: LUT Correction Value (P. 27)
TCS: Sensitivity Temperature Coefficient (P. 25)
ADMAX: Maximum Digital Value (P. 27)
ADMIN: Minimum Digital Value (P. 27)
OSADB: Offset Bulk AD Converter (P. 21)
OSADH: Offset Heater AD Converter (P. 22)
ENOCM: Internal test use only: program to ’1’
ENOCC: Internal test use only: program to ’1’

Error Monitor
CFGE: Error Bit Activation Mask (P. 28)

Temperature Sensor
OSTEMP: Temperature Offset Calibration (P. 29)
RTEMP: Reference Temperature (P. 29)
TEMPREF: Reference Temperature Source (P. 29)

EEPROM Interface
CRC_E2P: EEPROM Data Check Sum (P. 33)

REGISTER MAP (EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SELF AND SENSOR BIASING								
0x00	ADOS	ENREF	IBULK(1:0)		CFGIBN(3:0)			
TEMPERATURE SENSOR								
0x01				TEMPREF	OSTEMP(3:0)			
0x02	RTEMP(7:0)							
PI CONTROLLER								
0x03	RTCR	RAWAD	CMODE(1:0)		CIMAX(3:0)			
0x04	CKP(7:0)							
0x05	CKI(7:0)							
0x06	TCR(7:0)							
0x07	UB20(7:0)							
0x08					UB20(11:8)			
0x09	UH20(7:0)							
0x0A			UH20(13:8)					
0x0B	IHEAT(7:0)							
0x0C			RIHEAT	SWACT	IHEAT(11:8)			
0x0D	TSENSRD1(7:0)							
0x0E	TSENSRD2(7:0)							
0x0F		T1F(6:0)						
0x10	T1T(7:0)							
0x11		T2F(6:0)						
0x12	T2T(7:0)							
SENSOR SIGNAL CONDITIONING								
0x13	OS(3:0)				GAIN2(1:0)		GAIN1(1:0)	
0x14	REFOS	OS(10:4)						
0x15	TCOS(7:0)							
ERROR MONITOR								
0x16		CFGE(6:0)						
OPERATING MODE								
0x17	OPMODE(7:0)							
DIGITAL LINEARIZATION								
0x18	TCS(7:0)							
0x19	ADMIN(7:0)							
0x1A	ADMIN(15:8)							
0x1B	ADMAX(7:0)							
0x1C	ADMAX(15:8)							
0x1D	OSADB(7:0)							
0x1E	OSADH(7:0)							
0x1F	ENOCC	ENOCM	CHM(1:0)					
0x20	LUTA1(7:0)							
0x21	LUTA2(7:0)							
0x22	LUTA3(7:0)							
0x23	LUTA4(7:0)							

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x24	LUTA5(7:0)							
0x25	LUTA6(7:0)							
0x26	LUTA7(7:0)							
0x27	LUTA8(7:0)							
0x28	LUTD0(7:0)							
0x29	LUTD0(15:8)							
0x2A	LUTD1(7:0)							
0x2B	LUTD1(15:8)							
0x2C	LUTD2(7:0)							
0x2D	LUTD2(15:8)							
0x2E	LUTD3(7:0)							
0x2F	LUTD3(15:8)							
0x30	LUTD4(7:0)							
0x31	LUTD4(15:8)							
0x32	LUTD5(7:0)							
0x33	LUTD5(15:8)							
0x34	LUTD6(7:0)							
0x35	LUTD6(15:8)							
0x36	LUTD7(7:0)							
0x37	LUTD7(15:8)							
0x38	LUTD8(7:0)							
0x39	LUTD8(15:8)							
0x3A	LUTD9(7:0)							
0x3B	LUTD9(15:8)							
RESERVED RAM								
0x3C	reserved							
0x3D	reserved							
EEPROM INTERFACE								
0x3E	CRC_E2P(7:0)							
0x3F	CRC_E2P(15:8)							
STATUS REGISTER (read only registers)								
0x40	DSENS(7:0)							
0x41	DSENS(15:8)							
0x42			ERROR(5:0)					
0x43	DTEMP(7:0)							
0x44	THACT(7:0)							
0x45				THACT(12:8)				
0x46	TBACT(7:0)							
0x47						TBACT(10:8)		
0x48	OSACT(7:0)							
0x49							OSACT(9:8)	
0x4A	IHEATACT(7:0)							
0x4B					IHEATACT(11:8)			

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
iC IDENTIFIER (ROM)								
0x50	0x48 ≙ 'H'							
0x51	0x4F ≙ 'O'							
0x52	REV(7:0)							
0x53	0x69 ≙ 'i'							
0x54	0x43 ≙ 'C'							

Table 5: Register layout

OPERATING MODES AND CALIBRATION PROCEDURE

Operating Modes

iC-HO supports different sensors, providing both digital and analog output of the conditioned sensor signals. The following table gives the various modes of operation.

OPMODE	Addr. 0x17; bit 7:0	RW - 0x00
Code	Mode	Description
0x00	IDLE/RESET	default startup state
0x01	OPERATE	standard operation mode
0x02	CAL_UX20	calibration external resistors
0x03	WRITE_CONF	transfers internal config. data to EEPROM
0x04	MEAS_ANA	activates ADP/ADN output at OUTP/OUTN, IBN output at NERR
0x05	MEAS_CTRL	activates buffered HEATP/HEATN output at OUTP/OUTN
0x06	reserved	
...	...	
0xFF	reserved	

Table 6: Operating Modes

In mode **IDLE/RESET** all internal state machines and counters are reset. The configuration RAM is not reset here.

OPERATE is the standard operating mode.

Mode **CAL_UX20** performs the necessary reference measurement to be able to calculate the bulk and heater resistors temperature. Before evoking this command, it is necessary to set the resistor's temperature coefficient (parameter TCR table 26), to correct the internal thermometer offset (parameter OSTEMP table 44) and to calibrate the offsets of the bulk and heater analog to digital converters (parameter OSADB table 25 and OSADH table 28). After running **CAL_UX20** the heater resistor is biased with IHEATACT = 0x40, which corresponds to 560µA and does not heat up the heating resistor. The bulk resistor is biased with the set current (parameter IBULK table 11). Then the analog to digital converters reading UH and UB (see figure 2) is stored in the corresponding parameters UH20 and UB20. The actual temperature of the device (status register DTEMP table 45) is also stored as reference temperature in parameter RTEMP. With these parameters the iC-HO is able to calculate the temperature of both the heater and bulk resistor.

N.B.:
After changing parameter IBULK it is necessary to recall the **CAL_UX20** calibration routine. Otherwise the temperature calculation of the bulk resistor would fail.

N.B.:
RTEMP can be changed manually without affecting the calculation accuracy and characteristic curve of the temperature calculation. It can be seen as a constant offset to the temperature calculation.

UB20	Addr. 0x07; bit 7:0	
UB20	Addr. 0x08; bit 11:8	RW - 0x000
Code	Value	
0x000	0	
0x001	1	
...	...	
0xFFF	4095	

Table 7: Reference Bulk Resistor Reading

UH20	Addr. 0x09; bit 7:0	
UH20	Addr. 0x0A; bit 13:8	RW - 0x0000
Code	Value	
0x0000	0	
0x0001	1	
...	...	
0x3FFF	16383	

Table 8: Reference Heater Resistor Reading

MEAS_ANA serves for analog calibration. The internal nodes ADP and ADN are output. ADP is output at pin OUTP, ADN is output at pin OUTN. The internal bias current IBN is output via NERR.

Mode **MEAS_CTRL** is implemented for redesign version HO_Y and helps setting the optimal PI controller parameters. The voltages HEATP and HEATN are observable at the output pins OUTP and OUTN while the controller is working with the actually set parameters.

With **WRITE_CONF** the internal configuration is stored to the EEPROM. The CRC (CRC_E2P) is automatically updated and written to the EEPROM as well.

From redesign version HO_Z1 on, the operating mode of the analog-to-digital converters can be changed between optimized offset and optimized signal to noise performance. For version HO_Y 0x3 should be chosen as standard operation mode. This results in an optimized behavior in offset and noise performance as well.

CHM	Addr. 0x1F; bit 5:4 RW - 0x0
Code	Value
0x0	offset optimized
0x1	SNR optimized mode A
0x2	SNR optimized mode B
0x3	normal operation

Table 9: Analog-to-Digital Converter Mode

When using the signal to noise optimized mode A or B, the one with the lowest offset should be used for each device.

Calibration Procedure
The recommended calibration procedure is shown in the following figure.

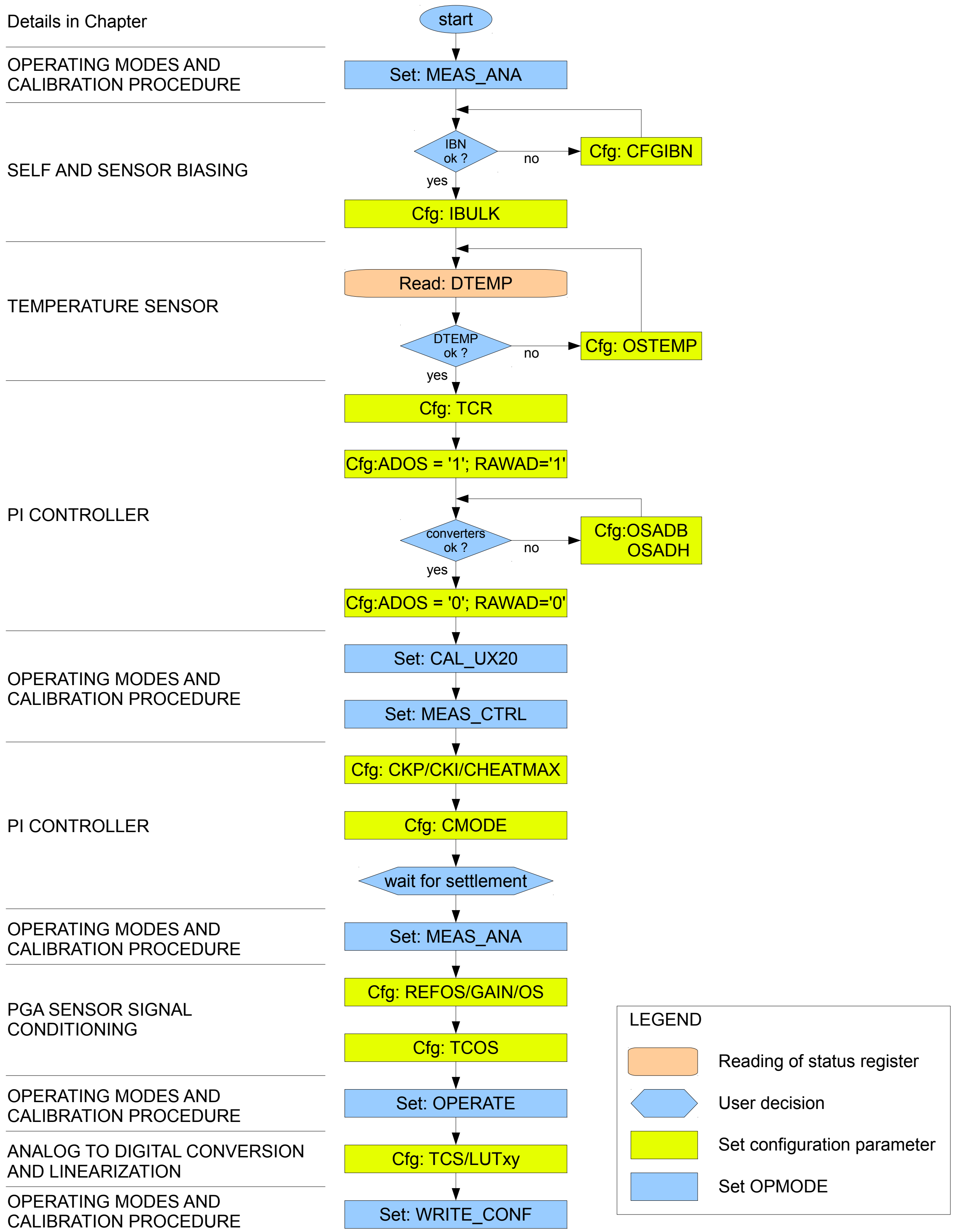


Figure 2: Calibration Procedure

STARTUP BEHAVIOR

After turning on the power supply (power-on reset) iC-HO reads the configuration data from the EEPROM. If the data can be read without error, a timeout of 1 ms is allowed to elapse. iC-HO then switches to normal operation.

If an error occurs while the EEPROM data is being read (a CRC error), the current reading process is restarted. Following a third failed attempt the reading procedure is stopped and the internal iC-HO configuration registers are initialized with its reset values. The EEPROM error bit is set.

SELF AND SENSOR BIASING

Bias Current Source

The calibration of the bias current source in operation mode **MEAS_ANA** is prerequisite for adherence to the given electrical characteristics and is also instrumental in the determination of the chip timing (e.g. internal clock frequency). The IBN current can be measured at pin NERR against GNDA. The set point for IBN is given in electrical characteristics A01.

CFGIBN	Addr. 0x00; bit 3:0 RW - 0x8
Code k	$IBN \sim \frac{31}{16+k}$
0x0	193.7 %
...	...
0xE	103.3 %
0xF	100.0 %

Table 10: Bias Current Source Calibration

Sensor Biasing

iC-HO is capable of biasing three resistors with a constant current. Outputs SUS1 and SUS2 are set to a fixed value and fit each other very well. Therefore these currents are intended for sensing element biasing. The third output SUS3 is configurable and though fits various bulk resistors.

IBULK	Addr. 0x00; bit 5:4 RW - 0x0
Code	I(SUS3)
0x0	-140 µA
0x1	-280 µA
0x2	-420 µA
0x3	-560 µA

Table 11: Current Output SUS3

Analog-to-Digital Converter Reference voltages

The internal reference voltages for the analog-to-digital converters have to be well blocked by external capacitors. It is possible to deactivate the internal buffers to externally feed those reference voltages with parameter ENREF.

ENREF	Addr. 0x00; bit 6 RW - 0x0
Code	status
0x0	buffers disabled
0x1	buffers enabled

Table 12: Enable Reference Buffers

Unused pins can be left open without further attention.

PI CONTROLLER

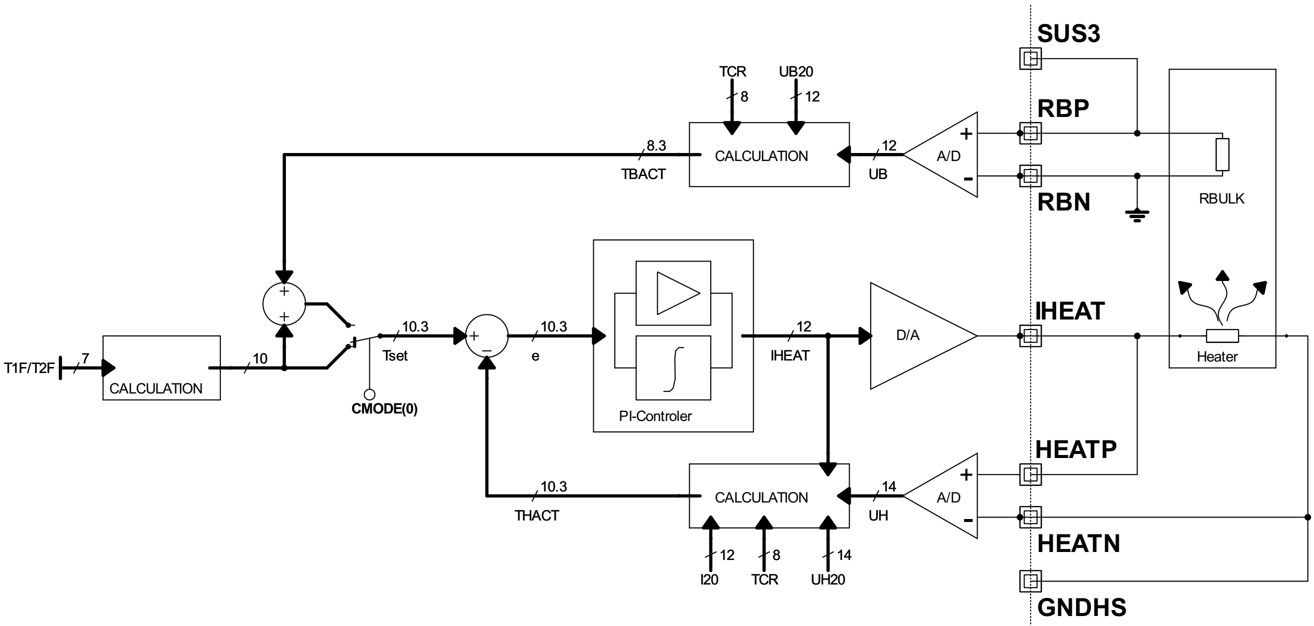


Figure 3: PI-Controller Overview

The PI controller circuit consists of two analog-to-digital converters, a digital-to-analog converter and a digitally implemented PI controller algorithm. With the two analog-to-digital converters the voltage drop over a bulk and a heater resistor is measured. With these two values and the stored reference values the actual temperature of both is calculated. Dependent on the selected mode the digital-to-analog converter is controlled to attain the temperature set point. There are four operating modes possible (table 13).

CMODE	Addr. 0x03; bit 5:4			RW - 0x0
Code	Controller Mode	A/D Converter Bulk	A/D Converter Heater	D/A Converter Heater
0x0	idle	running	idle	off
0x1	idle	running	running	constant current
0x2	offset	running	running	controlled
0x3	absolute	running	running	controlled

Table 13: Controller Operation Modes

With RAWAD it is possible to read the raw A/D converters outputs via the status registers. With that the linearization parameters and the Thresholds ADMIN/ADMAX can be set.

RAWAD	Addr. 0x03; bit 6 RW - 0x0
Code	Status Register Output
0x0	calculated TBACT, THACT and DSENS
0x1	A/D Converter Output UB, UH and RAWAD

Table 14: Output Multiplexer

Controller Mode
The controller can either be operated in temperature offset or absolute temperature mode (see table 13). In offset mode the reference temperature source will be set by TEMPREF (see table 47). The temperature set point is configured in T1F and T2F (see table 15). Further the corresponding time is set using T1T and T2T (see table 16). The controller starts with set point T1F for T1T seconds and then switches to set point T2F for T2T seconds. Then it continues alternating the two set points with the given timing scheme. If there is no need for alternating set points, T1F and T2F have to be set equal.

T1F	Addr. 0x0F; bit 6:0	RW - 0x00
T2F	Addr. 0x11; bit 6:0	RW - 0x00
Code	Temperature	
0x00	25 °C	
0x01	30 °C	
...	...	
0x7F	660 °C	

Table 15: Set Point T1/T2 Temperature

T1T(7:0)	Addr. 0x10; bit 7:0	RW - 0x00
T2T(7:0)	Addr. 0x12; bit 7:0	RW - 0x00
Code	Period	
0x00	100 ms	
0x01	200 ms	
...	...	
0xFF	25.6 s	

Table 16: Set Point T1/T2 Period

If necessary the heater can be switched to high impedance on pins HEATP and HEATN while reading and biasing the sensing element through pins VDDAS and GNDAS and vice versa. This is configured with parameter SWACT. This is not possible for the continuous reading mode defined by TSENSRD1 and TSENSRD2 equal to zero.

SWACT	Addr. 0x0C; bit 4	RW - 0x0
Code	mode	
0x0	standard	
0x1	Alternate Supply of Heater and Sensing Element	

Table 17: Activate Alternating Heater and Sensor Supply Switching

With TSENSRD1 and TSENSRD2 the sensor reading time points at SPIN and SNIN can be linked and synchronized to the controller timing. Further the data acquisition mode for the sensing element (page 25) is set by the combination of both parameters.

TSENSRD1(7:0)	Addr. 0x0D; bit 7:0	RW - 0x000
Code	time point	
0x00	special mode (see table 20)	
0x01	100 ms	
0x02	200 ms	
...	...	
0xFF	25.5 s	
Constraint	T1T+T2T > TSENSRD1	

Table 18: Sensor Read Time 1

TSENSRD2(7:0)	Addr. 0x0E; bit 7:0	RW - 0x000
Code	time point	
0x00	special mode (see table 20)	
0x01	100 ms	
0x02	200 ms	
...	...	
0xFF	25.5 s	
Constraint	T1T+T2T > TSENSRD2	
Constraint	TSENSRD2 > TSENSRD1	

Table 19: Sensor Read Time 2

The data acquisition mode is affected as follows:

TSENSRD1	TSENSRD2	mode
= 0x00	= 0x00	continuous reading (for update rate see characteristics 202)
> 0x00	= 0x00	single measure at TSENSRD1
> 0x00	> 0x00	double measure at TSENSRD1 and TSENSRD2, RAWADS is calculated as the difference between reading at TSENSRD2 - TSENSRD1

Table 20: Sensing Element Data Acquisition Mode

When in absolute temperature mode the set point value Tset (see figure 3) is directly taken from T1F/T2F. If driven in offset temperature mode TBACT (see table 24) is added to the set point of the PI controller.

Controller Setup

CKP	Addr. 0x04; bit 7:0	RW - 0x00
Code	Factor	
0x00	0	
0x01	1	
...	...	
0xFF	255	

Table 21: Controller KP Parameter

CKI	Addr. 0x05; bit 7:0	RW - 0x00
Code	Factor	
0x00	0	
0x01	8	
...	...	
0xFF	2040	

Table 22: Controller KI Parameter

A/D Converter Calibration

For offset calibration of the analog-to-digital converters the currents flowing out of SUS3 and IHEAT can be programmed to zero with ADOS.

ADOS	Addr. 0x00; bit 7 RW - 0x0
Code	Mode
0x0	Normal Operation
0x1	IHEAT and SUS3 current is zero

Table 23: Disable SUS3/IHEAT Current Source

A/D Converter Bulk

The 12-bit analog voltage to digital converter converts the voltage drop over the bulk resistor between pins RBP (upper node) and RBN (lower node). With the stored reference voltage at 20 °C UB20 (12-bit, see table 7) and the configured resistor's temperature coefficient (parameter TCR and RTCR, see table 26) the actual bulk resistor's temperature is calculated. This fixed-point value is observable via SPI (parameter TBACT). The upper 8-bit represent the integer value and are coded as DTEMP (see table 45). The lower 3 bit represent the fractional part.

TBACT(7:0) **TBACT(10:8)**	Addr. 0x46; bit 7:0 Addr. 0x47; bit 2:0 R
Code	Temperature
0x000	-62.000 °C
0x001	-61.875 °C
...	...
0x7FF	193.875 °C

Table 24: Actual Bulk Resistor Temperature

The offset of the converter can be calibrated by parameter OSADB. Therefore ADOS should be set to 0x1 and RAWAD to 0x1.

N.B.:
With this configuration the analog to digital converters reading UH can be read in the status register THACT (see table 27). The current flowing through the heater resistor is configured to zero. So the read voltage drop UH needs be configured to zero with parameter OSADH (see table 28).

N.B.:
When calibrating UH to zero, take care not to overcompensate into negative values. As UH is an unsigned value, the correction with OSADH can be set to a negative value for UH without a possibility to detect externally.

OSADB(7:0)	Addr. 0x1D; bit 7:0 RW - 0x00
Code	offset [LSB]
0x00	0
0x01	1
...	...
0x7F	127
0x80	-128
0x81	-127
...	...
0xFF	-1

Table 25: Offset Bulk Resistor Converter

RTCR **TCR**	Addr. 0x03; bit 7 RW - 0x0 Addr. 0x06; bit 7:0 RW - 0x00	
Code RTCR	Code TCR	temperature coefficient
0	0x00	1953.125 ppm/°C
0	0x01	1956.939 ppm/°C
0	...	...
0	0xFF	2925.872 ppm/°C
1	0x00	2929.687 ppm/°C
1	0x01	2933.502 ppm/°C
1	...	...
1	0xFF	3902.435 ppm/°C

Table 26: Resistor Temperature Coefficient

A/D Converter Heater

This 14 bit analog voltage to digital converter converts the voltage drop over the heater resistor between pins HEATP (upper node) and HEATN (lower node). With the stored reference voltage at 20 °C UH20 (14 bit, see table 8) and the configured resistor's temperature coefficient (parameter TCR, see table 26) the actual heater resistor's temperature is calculated. This fixed-point value is observable via SPI (parameter TBACT see table 24). The upper 10 bit represent the integer value and are coded based on DTEMP (see table 45). The lower 3 bit represent the fractional part.

THACT(7:0) **THACT(12:8)**	Addr. 0x44; bit 7:0 Addr. 0x45; bit 4:0 R
Code	Temperature
0x0000	-62.000 °C
0x0001	-61.875 °C
...	...
0x1FFF	961.875 °C

Table 27: Actual Heater Resistor Temperature

The offset of the converter can be calibrated by parameter OSADH.

N.B.:
With this configuration the analog to digital converters reading UB can be read in the status register TBACT (see table 27). The current flowing through the heater resistor is configured to zero. So the read voltage drop UB, should be configured to zero with parameter OSADB (see table 25).

N.B.:
When calibrating UB to zero, take care not to overcompensate into negative values. As UB is an unsigned value, the correction with OSADB can be set to a negative value for UB without a possibility to detect externally.

Therefore ADOS should be set to 0x1 and RAWAD to 0x1 either.

OSADH(7:0) Addr. 0x1E; bit 7:0 RW - 0x00	
Code	offset [LSB]
0x00	0
0x01	1
...	...
0x7F	127
0x80	-128
0x81	-127
...	...
0xFF	-1

Table 28: Offset Heater Resistor Converter

D/A Converter Heater
The 12-bit digital to analog converter outputs a current flowing out of pin HEATP. Depending on parameter CMODE (table 13) it is constantly settable with parameter IHEAT (table 29) or controlled by the PI controllers output. The actual value is observable via IHEATACT.

IHEAT(7:0) Addr. 0x0B; bit 7:0 **IHEAT(11:8)** Addr. 0x0C; bit 11:8 RW - 0x000 **IHEATACT(7:0)** Addr. 0x4A; bit 7:0 **IHEATACT(11:8)** Addr. 0x4B; bit 11:8 R	
Code	Current
0x000	0 µA
0x001	8.75 µA
...	...
0xFFF	35.83 mA

Table 29: HEATP Current

In order to save the heater resistor, the PI controller's output can be limited by CIMAX to a maximum value.

CIMAX Addr. 0x03; bit 3:0 RW - 0xF	
Code	Current
0x0	2.23 mA
0x1	4.47 mA
0x2	6.71 mA
...	...
0xF	35.83 mA

Table 30: Maximum PI Controller Output Current

In order to extend the current output from revision HO_Y on, RIHEAT doubles the output current. This parameter must not be changed after calibration. You need to take into account that the CIMAX values are also doubled.

RIHEAT Addr. 0x0C; bit 5 RW - 0x0	
Code	Mode
0x0	Normal Operation
0x1	Double IHEAT Current

Table 31: Heater Current Range

PGA SENSOR SIGNAL CONDITIONING

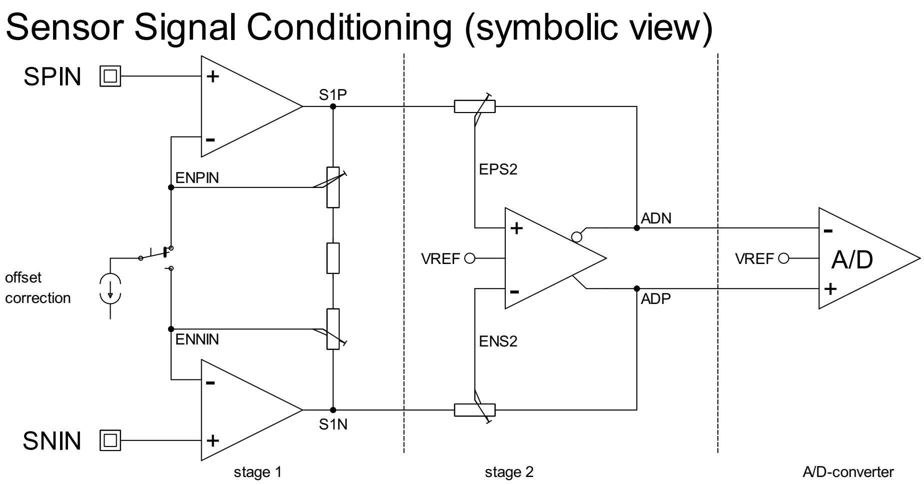


Figure 4: Symbolic View of the PGA Input Circuit

The sensor signal input stage is an instrumentation PGA architecture. Amplification and offset can be calibrated. Amplification is set using parameters GAIN1 and GAIN2. GAIN1 sets the amplification for stage 1 and GAIN2 for stage 2.

GAIN1		Addr. 0x13; bit 1:0		RW - 0x0
GAIN2		Addr. 0x13; bit 3:2		RW - 0x0
Code GAIN1	Code GAIN2	AV_{tot}	AV_{stage1}	AV_{stage2}
0x0	0x0	1.1	1.1	1
0x1	0x0	2	2	1
0x2	0x0	3	3	1
0x3	0x0	4	4	1
0x0	0x1	3.3	1.1	3
0x1	0x1	6	2	3
0x2	0x1	9	3	3
0x3	0x1	12	4	3
0x0	0x2	5.5	1.1	5
0x1	0x2	10	2	5
0x2	0x2	15	3	5
0x3	0x2	20	4	5
0x0	0x3	13.2	1.1	12
0x1	0x3	24	2	12
0x2	0x3	36	3	12
0x3	0x3	48	4	12

Table 32: PGA Amplification

The calibration range for the offset is dependent on the source selected by REFOS and is set using parameter OS. With parameter REFOS it is possible to select a constant offset or ratiometric offset calibration.

REFOS	Addr. 0x14; bit 7	RW - 0x0
Code	Type of source	
0	Feedback of pin VDDA	REFVOS = $\frac{V(VDDA)}{50}$
1	Reference V100	REFVOS = 100 mV

Table 33: Offset Reference Source

The sensors offset is calibrated by a linear voltage divider using OS(10:0).

OS(3:0)	Addr. 0x13; bit 7:4	
OS(10:4)	Addr. 0x14; bit 6:0	RW - 0x000
Code	$VOS = cOS \times REFVOS$	
0x000	cOS = 0	
0x001	cOS = -0.0009	
0x002	cOS = -0.0019	
0x003	cOS = -0.0029	
...	...	
0x3FF	cOS = -0.9990	
0x400	cOS = 0	
0x401	cOS = 0.0009	
0x402	cOS = 0.0019	
0x403	cOS = 0.0029	
...	...	
0x7FF	cOS = 0.9990	

Table 34: Offset Voltage

For temperature dependent offset values it is possible to dynamically track the OS value. The calibration reference temperature and the temperature coefficient has to be set. The default value for the temperature coefficient is zero which turns off the dynamical tracking. To set the reference temperature see chapter TEMPERATURE SENSOR (table 46).

TCOS	Addr. 0x15; bit 7:0 RW - 0xC5
Code	Tc(OS)
0x00	-6012.000 ppm/°C
...	...
0xC5	0.0 ppm/°C
0xC6	30.52 ppm/°C
...	...
0xFF	1770 ppm/°C

Table 35: Temperature Coefficient Offset Voltage

The actual calculated absolute offset correction value OSACT is readable in the status register.

OSACT(7:0)	Addr. 0x48; bit 7:0
OSACT(9:8)	Addr. 0x49; bit 1:0 R
0x000	$\lvert cOS \rvert = 0$
0x001	$\lvert cOS \rvert = 0.0009$
...	...
0x3FF	$\lvert cOS \rvert = 0.9990$

Table 36: Actual Absolute Offset Correction

The resulting offset correction depends on the gain settings as shown in the following table.

Av_{tot}	PGA output offset calibration	input referenced offset calibration
1.1	$0.36 \times VOS$	$0.33 \times VOS$
2	$2 \times VOS$	$1 \times VOS$
3	$2.7 \times VOS$	$0.89 \times VOS$
3.3	$1.1 \times VOS$	$0.33 \times VOS$
4	$3 \times VOS$	$0.75 \times VOS$
5.5	$1.8 \times VOS$	$0.33 \times VOS$
6	$6 \times VOS$	$1 \times VOS$
9	$8 \times VOS$	$0.89 \times VOS$
10	$10 \times VOS$	$1 \times VOS$
12	$9 \times VOS$	$0.75 \times VOS$
13.2	$4.4 \times VOS$	$0.33 \times VOS$
15	$13.3 \times VOS$	$0.89 \times VOS$
20	$15 \times VOS$	$0.75 \times VOS$
24	$24 \times VOS$	$1 \times VOS$
36	$32 \times VOS$	$0.89 \times VOS$
48	$36 \times VOS$	$0.75 \times VOS$

Table 37: Offset Calibration Dependency on Gain Setting

ANALOG TO DIGITAL CONVERSION AND LINEARIZATION

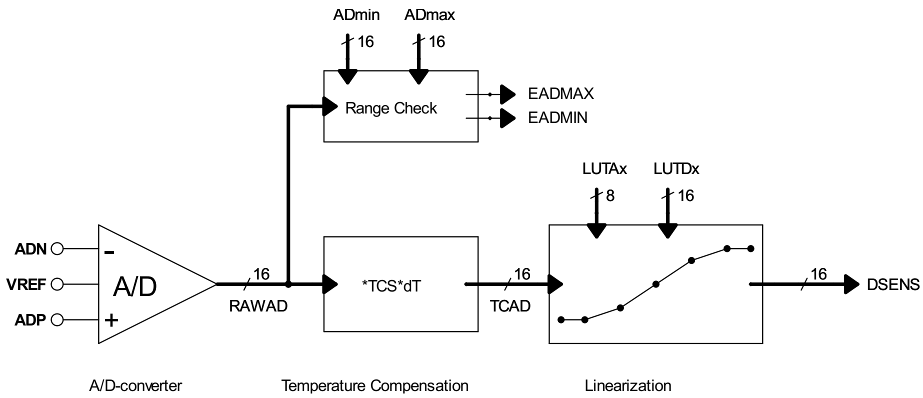


Figure 5: Analog to Digital Converter Overview

Analog to Digital Conversion

iC-HO contains an analog to digital converter with 16 bit resolution. The allowed conversion boundaries (see characteristics 205) represent 20% up to 80% full scale reading. RAWAD is either the analog to digital converters output directly or already the difference between two conversions. For more details on this operation mode refer to the PI controller section (table 20).

Sensitivity Temperature Compensation

For sensitivities temperature compensation the temperature coefficient TCS determines the correction factor.

TCS	Addr. 0x18; bit 7:0 RW - 0x00
Code	sensitivity temperature coefficient
0x00	0.0 ppm/°C
0x01	15.2 ppm/°C
...	...
0x7F	1937.9 ppm/°C
0x80	-1953.1 ppm/°C
...	...
0xFF	-15.2 ppm/°C

Table 38: Sensitivity Temperature Coefficient

Therefore the reference temperature has to be set see chapter TEMPERATURE SENSOR (table 46).

Linearization

A piece-wise linear interpolation of values stored in a look-up-table (LUT) is employed to calculate the gain and offset for a given analog to digital converters output TCAD (see figure 5 and 6). These calculations are changed from version HO_Y so please read the manual carefully.

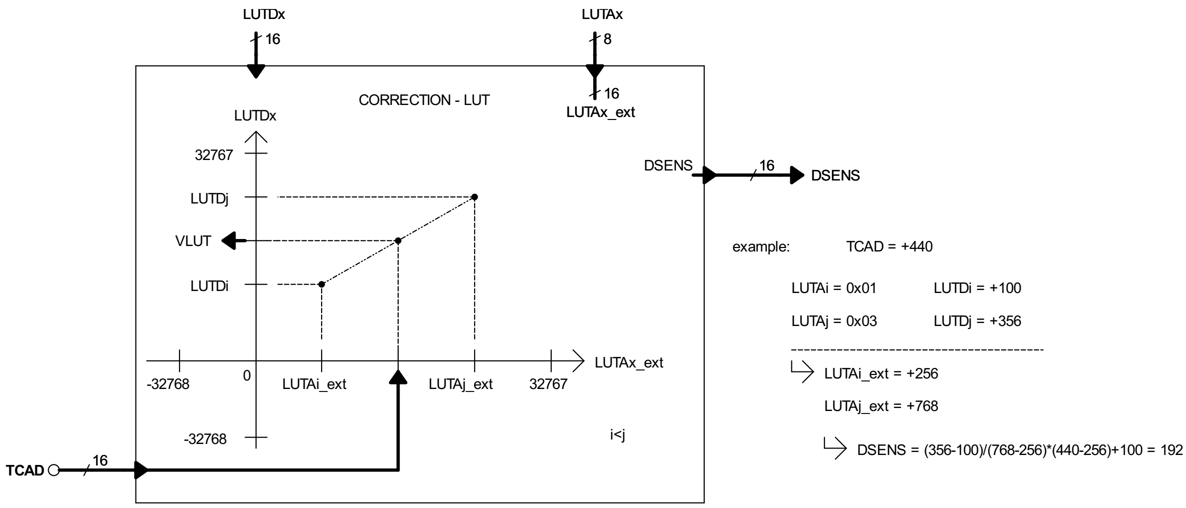


Figure 6: detailed linearization drawing

There can be a minimum of two up to a maximum of ten breakpoints within the LUT. Each breakpoint can be addressed with 8 bit resolution.

LUTA0_ext	defined as -32768	
LUTA1	Addr. 0x20; bit 7:0	RW - 0x00
LUTA2	Addr. 0x21; bit 7:0	RW - 0x00
LUTA3	Addr. 0x22; bit 7:0	RW - 0x00
LUTA4	Addr. 0x23; bit 7:0	RW - 0x00
LUTA5	Addr. 0x24; bit 7:0	RW - 0x00
LUTA6	Addr. 0x25; bit 7:0	RW - 0x00
LUTA7	Addr. 0x26; bit 7:0	RW - 0x00
LUTA8	Addr. 0x27; bit 7:0	RW - 0x00
LUTA9_ext	defined as 32767	

Code	16 bit breakpoint address
0x81	-32512
0x82	-32256
...	...
0xFF	-256
0x00	0
0x01	256
...	...
...	...
0x7E	32256
0x7F	32512
0x80	32767 (by definition)

Table 39: LUT Address Breakpoints

Breakpoints can be placed freely across the analog to digital converters output range except for the first and the last breakpoint. The first breakpoint LUTA0_ext is fixed at the minimum ADC value (-32768), the last breakpoint LUTA9_ext is fixed at the maximum ADC value (32767). Addresses must be stored in increasing order. An address of 0x80, which is defined to be the maximum ADC value, marks the last valid LUT entry. All addresses thereafter including their data value (LUTDx) will be ignored.

Each breakpoint has a data value in two's complement representation associated to it. Data values must be monotonically increasing, identical values are allowed.

LUTD0(7:0)	Addr. 0x28; bit 7:0	
LUTD0(15:8)	Addr. 0x29; bit 7:0	RW - 0x000
LUTD1(7:0)	Addr. 0x2A; bit 7:0	
LUTD1(15:8)	Addr. 0x2B; bit 7:0	RW - 0x000
LUTD2(7:0)	Addr. 0x2C; bit 7:0	
LUTD2(15:8)	Addr. 0x2D; bit 7:0	RW - 0x000
LUTD3(7:0)	Addr. 0x2E; bit 7:0	
LUTD3(15:8)	Addr. 0x2F; bit 7:0	RW - 0x000
LUTD4(7:0)	Addr. 0x30; bit 7:0	
LUTD4(15:8)	Addr. 0x31; bit 7:0	RW - 0x000
LUTD5(7:0)	Addr. 0x32; bit 7:0	
LUTD5(15:8)	Addr. 0x33; bit 7:0	RW - 0x000
LUTD6(7:0)	Addr. 0x34; bit 7:0	
LUTD6(15:8)	Addr. 0x35; bit 7:0	RW - 0x000
LUTD7(7:0)	Addr. 0x36; bit 7:0	
LUTD7(15:8)	Addr. 0x37; bit 7:0	RW - 0x000
LUTD8(7:0)	Addr. 0x38; bit 7:0	
LUTD8(15:8)	Addr. 0x39; bit 7:0	RW - 0x000
LUTD9(7:0)	Addr. 0x3A; bit 7:0	
LUTD9(15:8)	Addr. 0x3B; bit 7:0	RW - 0x000

Code	data value
0x8000	-32768
0x8001	-32767
...	...
0xFFFF	-1
0x0000	0
0x0001	1
...	...
0x7FFF	32767

Table 40: LUT Data Value

Characteristic dependent linearization is performed by linear interpolation between breakpoints. If a linearization is undesired the value of LUTA1 has to be set to 0x80, LUTD0 to 0x8000 and LUTD1 to 0x7FFF. The processed upper 10 bit are output as DSENS to the digital to analog converter and the status register (see table 48).

Two threshold values can be defined as a minimum analog to digital converters reading (ADMIN) or as maximum (ADMAX). If one of these thresholds is exceeded the corresponding error bit EADMIN or EADMAX is set. They both refer to the unprocessed 16 bit analog to digital converters output.

ADMIN(7:0)	Addr. 0x19; bit 7:0	
ADMIN(15:8)	Addr. 0x1A; bit 7:0	RW - 0x0000
ADMAX(7:0)	Addr. 0x1B; bit 7:0	
ADMAX(15:8)	Addr. 0x1C; bit 7:0	RW - 0x0000

Code	threshold value
0x8000	-32768
0x8001	-32767
...	...
0xFFFF	-1
0x0000	0
0x0001	1
...	...
0x7FFF	32767

Table 41: Error Threshold Value

ERROR MONITOR

iC-HO provides several possibilities to monitor errors. If an error occurs the open drain output pin NERR is pulled down and the respective error bit in the status register is set. The error bits are maintained until the status register is read out.

ERROR	Addr. 0x42; bit 5:0	R
Bit	name	meaning
0	EHEATBD	heater breakdown when high impedance is detected at pin HEATP
1	EHEATSC	heater short-circuit when the PI controller is active. Otherwise EHEATSC is always off
2	ESENSBD	Sensor or bulk resistor breakdown when the sensor is biased by SUS1/SUS2/SUS3. Each of the active sources (defined by CFGE(4:2)) can activate the error bit
3	EADMAX	sensor output above ADMAX
4	EADMIN	sensor output below ADMIN
5	EEEPROM	EEPROM not present or invalid (CRC)

Table 42: Error Description

It is possible to disable some of these error bits by a configuration mask (see table 43). If an error bit is deactivated it also does not pull down pin NERR.

CFGE	Addr. 0x16; bit 6:0 RW - 0x00
Bit	**status for error bit**
0	EHEATBD
1	EHEATSC
2	ESENSBD/SUS1
3	ESENSBD/SUS2
4	ESENSBD/SUS3
5	EADMAX
6	EADMIN
	Encoding of bit 4...0: 1 = error check enabled, 0 = error check disabled

Table 43: Error Bit Configuration

TEMPERATURE SENSOR

iC-HO includes an internal digital 8 bit temperature sensor. Its offset can be calibrated by the parameter OSTEMP.

OSTEMP	Addr. 0x01; bit 3:0 RW - 0x0
Code	Temperature Correction
0x8	-8 °C
0x9	-7 °C
0xA	-6 °C
0xB	-5 °C
0xC	-4 °C
0xD	-3 °C
0xE	-2 °C
0xF	-1 °C
0x0	0 °C
0x1	1 °C
0x2	2 °C
0x3	3 °C
0x4	4 °C
0x5	5 °C
0x6	6 °C
0x7	7 °C

Table 44: Temperature Sensor Offset

The digital temperature representation DTEMP is stored in the status register and is mapped in table 45.

DTEMP	Addr. 0x43; bit 7:0 R
Code	Temperature
0x00	-62 °C
0x01	-61 °C
...	...
0x16	-40 °C
...	...
0x3E	0 °C
...	...
0x52	20 °C
...	...
0xA2	100 °C
...	...
0xFF	193 °C

Table 45: Temperature Sensor Value Representation

For digital linearization of the temperature dependent sensor characteristic (see DIGITAL LINEARIZATION, page **??**) and temperature dependent analog offset calibration (see PGA SENSOR SIGNAL CONDITIONING, page 23) the calibration temperature has to be stored as reference value RTEMP for the mentioned calculations. This is done automatically when evoking *CAL_UX20*. The digital value representation is identical to parameter DTEMP (table 45).

RTEMP	Addr. 0x02; bit 7:0 RW - 0x00
Code	Temperature
0x00	-62 °C
0x01	-61 °C
...	...
0x16	-40 °C
...	...
0x3E	0 °C
...	...
0x52	20 °C
...	...
0xA2	100 °C
...	...
0xFF	193 °C

Table 46: Reference Temperature Value Representation

iC-HO can perform the mentioned temperature compensations referred to the integrated thermometer taking into account the temperature difference between DTEMP and RTEMP or referred to the external bulk thermometer taking into account the temperature difference between TBACT(11:4) and RTEMP. TEMPREF selects the reference.

TEMPREF	Addr. 0x01; bit 4 RW - 0x0
Code	source
0x0	integrated thermometer
0x1	external bulk resistor

Table 47: Temperature Compensation Source

ANALOG OUTPUT

The 10 bit digital to analog converter with ratiometric differential analog output pins are OUTP and OUTN. The conditioned status register value DSENS (see page 27) is the converters digital source. The most significant 10 bit are used for the converter. The DA converter is active in operation mode *OPERATE*.

STATUS REGISTER

The status register starts at address 0x40 up to 0x4B. Digital sensor data output, error messages, temperature and status information can be read.

STATUS	Addr. 0x40-0x4B;		R
Name	Starting address	Ending address	Reference
DSENS	0x40	0x41	see figure 5
ERROR	0x42	0x42	table 42
DTEMP	0x43	0x43	table 45
THACT	0x44	0x45	table 27
TBACT	0x46	0x47	table 24
OSACT	0x48	0x49	table 36
IHEATACT	0x4A	0x4B	table 29

Table 48: Status Register

SPI SLAVE INTERFACE

The SPI slave interface can be used to access the iC-HO directly by a microcontroller or any other type of host.

SPI name	pin name	description
NCS	NCS_S	not chip select
SCLK	SCK_S	clock
MOSI	MOSI_S	master out slave in
MISO	MISO_S	master in slave out

Table 49: SPI Connector Pin List

The SPI modes 0 and 3 are supported, i.e. an idle polarity of SCLK 0 or 1 and acceptance of data with a rising edge of SCLK.

The idle level of the MISO line is tristate. (Tristate MIS-O-Output is not implemented in the first version HO_0). The slave passes MOSI to MISO on a falling edge at NCS.

Data is sent byte wise with the MSB first. Each data transmission begins with the master sending an opcode. To be compatible to Microwire™, all opcodes start with a 1.

OPCODEs	
Code	Description
0x8A	Read REGISTER (cont.)
0xCF	Write REGISTER (cont.)
0xAD	REGISTER status/data
0x9C	Read STATUS
0xD9	Write INSTRUCTION

Table 50: OPCODE table

The **REGISTER status/data** command can be used to request the status of the last register communication and/or the last data transmission. The SPISTATUS byte contains the information summarized in Table 51.

SPISTATUS		
Bit	Name	Description of the status report
6..4	-	Reserved
3	DISMISS	Address refused
2	FAIL	Data request has failed
1	BUSY	Slave is busy with a request
0	VALID	DATA is valid
NB	Display logic: 1 = true, 0 = false	

Table 51: Communication Status Byte

All status bits are updated with each register access. The exception to the rule is the ERROR bit; this bit indicates whether an error occurred during the last SPI communication with the slave.

The master transmits the **REGISTER status/data** op-code. The slave immediately passes the opcode on to MISO. The slave then transmits the STATUS byte and a DATA byte. The DATA byte is undefined in the actual configuration.

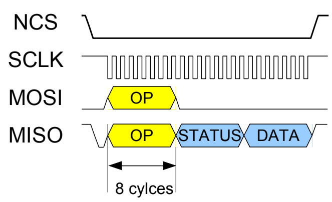


Figure 7: REGISTER status/data

Read REGISTER (cont.)
For reading data from internal registers the slave does not need any processing time. These registers can be read out in continuous mode.

The master transmits the **Read REGISTER (cont.)** op-code. In the second byte the start address ADR is transmitted. The slave immediately outputs the opcode, address and then transmits the DATA1 data. The internal address counter is incremented following each data byte.

If an error occurs during register readout in continuous mode (e.g. the address is invalid or the requested data is not yet valid on data byte clockout), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register (see page 31).

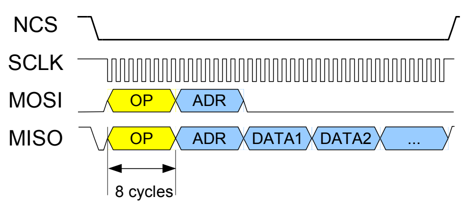


Figure 8: Read REGISTER (cont.)

Write REGISTER (cont.)

For writing data into internal registers the slave does not need any processing time. These registers can be written in continuous mode.

The master transmits the **Write REGISTER (cont.)** opcode. In the second byte start address ADR is transmitted, followed by the data bytes (DATA1-DATAn) to be written. The slave immediately outputs the opcode, address, and data at MISO. The slave increments its internal address counter following each data byte.

If an error occurs during write to register in continuous mode (e.g. the address is invalid or the data write process of the last address was not finished), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register (see page 31).

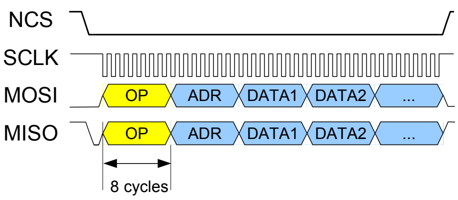


Figure 9: Write REGISTER (cont.)

Read STATUS

The command **Read STATUS** is designed to enable a fast readout of the internal iC-HO status registers (STATUS, table 48). The opcode sets the address in the slave to the lowest STATUS address. The internal address counter is incremented following each status byte. This command largely corresponds to the Read REGISTER (cont.) command, with the difference that here the addressing sequence is missing and the master does not need to know the slaves exact STATUS address.

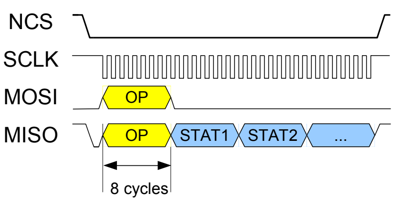


Figure 10: Read STATUS

Write INSTRUCTION

The command **Write INSTRUCTION** is designed to enable a fast setting of the iC-HO command register. The opcode sets the address in the slave to the command register address. The instruction data (OPMODE, see 6) follows as second byte. This command largely corresponds to the **Write REGISTER (cont.)** command, with the difference that here the addressing sequence is missing and the master does not need to know the slaves exact opcode address.

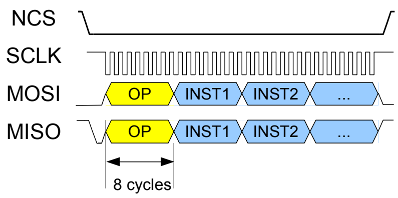


Figure 11: Write INSTRUCTION

DEVICE IDENTIFICATION

The device and device revision is identifiable with read only registers in the address range 0x50 . . . 0x54. See table 5 on page 14 section "iC IDENTIFIER (ROM)" for the revision independent part.

REV	Addr. 0x52; bit 7:0 R
Code	Description
0x00	iC-HO_0
0x01	iC-HO_1
0x02	iC-HO_Z
0x03	iC-HO_Z1
0x05	iC-HO_Y
0x06	iC-HO_Y1

Table 52: Device Revision

SPI EEPROM INTERFACE

The implemented SPI master is compatible with SPI serial EEPROMs that are compatible to ST95010.

SPI name	pin name	description
NCS	NCS_M	not chip select
SCK	SCK_M	clock
MOSI	MOSI_M	master out slave in
MISO	MISO_M	master in slave out

Table 53: SPI EEPROM Connector Pin List

Implemented are read and write command.

The data in the EEPROM is secured by a CRC to the addresses 0x35 and 0x36.

CRC_E2P(7:0) **CRC_E2P(15:8)**	Addr. 0x35; bit 7:0 Addr. 0x36; bit 15:8 R - 0x0000
Code	Description
0x0000 . . . 0xFFFF	CRC formed by CRC polynomial 0x11021

Table 54: EEPROM Data Check Sum

APPLICATION NOTES

TYPICAL BASIC SETUP

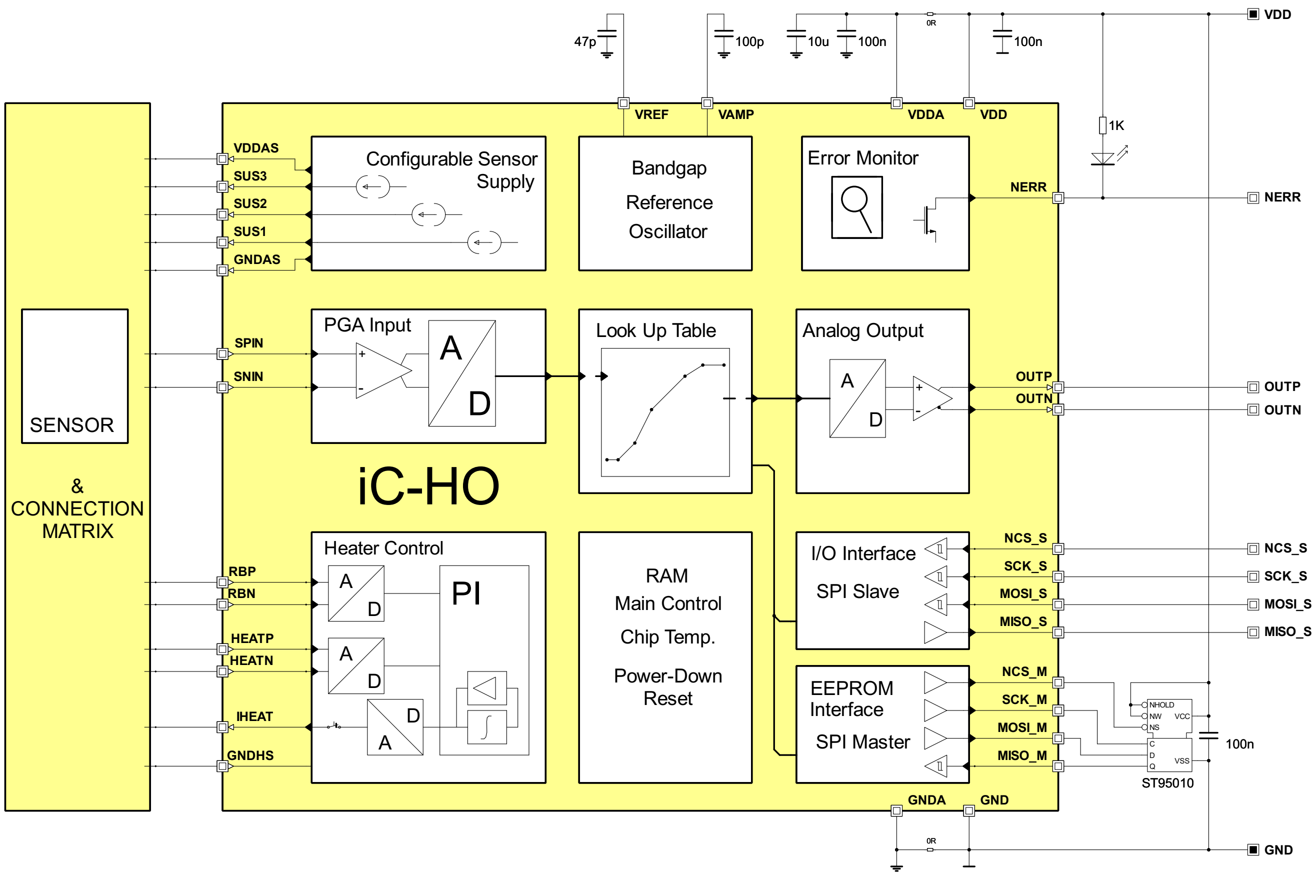


Figure 12: iC-HO basic setup schematic

SENSOR APPLICATIONS

This overview indicates typical sensor applications. Additionally needed passive components (blocking capacitors etc.) are not shown.

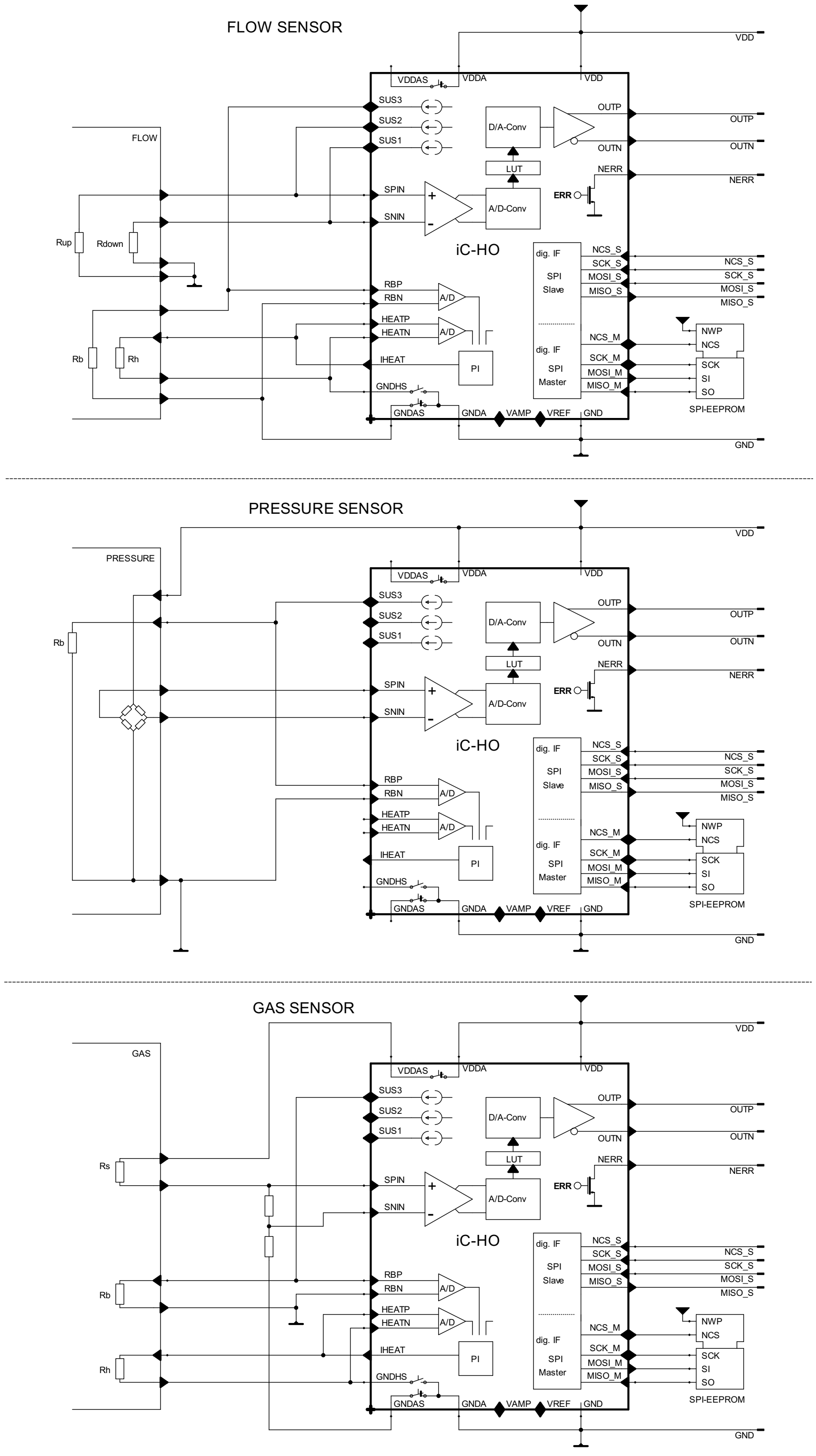


Figure 13: application schematics

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2018-11-22		Initial release	all

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-HO	32 pin QFN, 5 mm x 5 mm	iC-HO QFN32-5x5
Evaluation Board	100 mm x 80 mm	iC-HO EVAL HO1D

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