iC-GD
UNIVERSAL I/O INTERFACE

preliminary

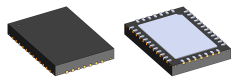
FEATURES

- Two channels, each configurable as input or output
- Low-side and high-side switches with up to 500 mA per channel, current limitation, current measurement, status messages, cable break detection, freewheeling and reverse polarity protection, paralleling of both channels possible
- Output of ±10 V or 0/4...20 mA with 14 bit resolution
- Measurement of ±10 V, ±1 V, ±100 mV, ±10 mV, ±20 mA, 4...20 mA with 14 bit resolution
- Input for Pt100, Pt1000 temperature sensors
- Multifunctional 32 bit counter
- Digital output with pulse-width modulation option
- Internal temperature measurement with 1 K resolution
- SPI interface
- Calibration and configuration by external EEPROM via serial interface
- Error message with hysteresis at overtemperature, overload and undervoltage
- Shutdown of the outputs in case of error
- Inputs/outputs protected against ESD

APPLICATIONS

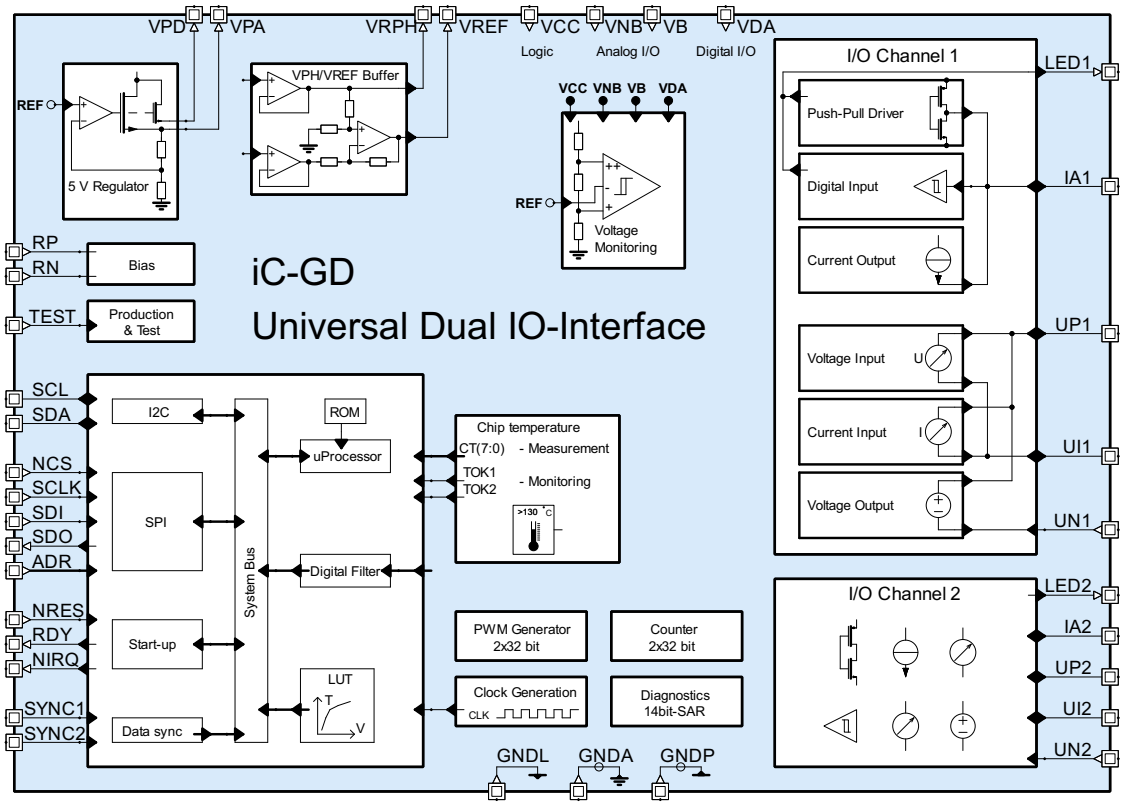
- PLC control systems
- Data acquisition
- Sensor interfaces

PACKAGES



QFN38 5 mm x 7 mm

BLOCK DIAGRAM



DESCRIPTION

iC-GD is an interface IC with two independent channels each of which is configurable for a variety of measurement and control signal transmission tasks.

Both channels, each with 4 pins, can be addressed via the SPI interface and configured by an external EEPROM or SPI.

When configured as low-side or high-side drivers, each channel is capable of high driving currents (at least 500 mA) with integrated current measurement and current limitation. Drivers are short-circuit proof by shut-down in case of overtemperature or overload.

The high/low-side drivers can be connected in parallel for higher currents and feature an active freewheeling circuit and reverse polarity protection.

Operated as an analog output, the iC-GD provides voltages in the range of ±10 V or currents in the range of 0 or 4 to 20 mA with a resolution of 14 bits.

When configured as an analog input, a 14-bit ADC processes differential voltages in the range of ±10 V, ±1 V, ±100 mV, ±10 mV or currents in the range of ±20 mA or 4 to 20 mA.

The analog inputs can be bandwidth-limited over a wide range from 2 kHz to 0.5 Hz by means of a configurable input filter. Additionally a *fast mode* with an 8 kHz limit is available.

Pt temperature sensors (in 2-, 3- and 4-wire technology) and various thermocouples can also be connected to provide the absolute temperature with a resolution of 0.1 K after calibration.

After calibration an integrated temperature sensor also supplies the absolute chip temperature with a resolution of 1 K.

In digital input mode, two 32-bit counters are available which can be configured for counting direction, start value, end value or used in combination as a single gated counter. An LED signals the state of the digital input even without the iC-GD being powered.

The digital output can be operated as a pulse-width modulator with a resolution of either 125 ns or 16 µs and a cycle time of up to 8.192 ms or 1.048 s.

If all pins of a channel are not used, it is possible to use certain functions of a channel simultaneously. Thus, for example, the high-side or low-side driver or the digital input respectively can be operated independent of voltage and current measurement or voltage output.

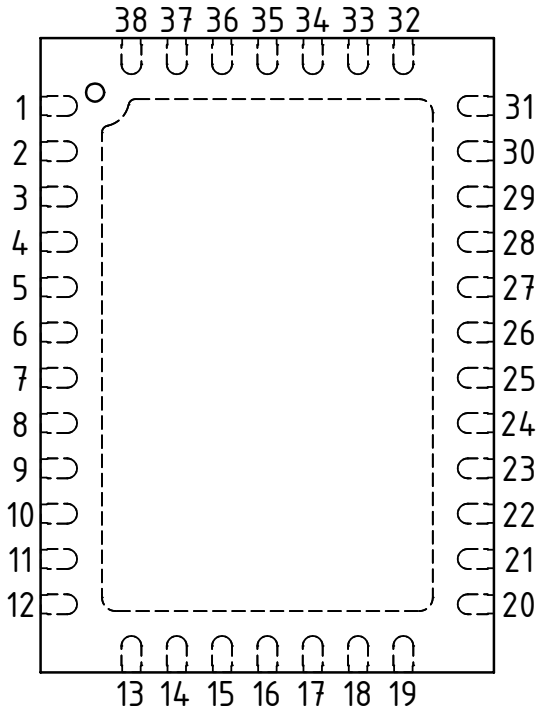
A variety of monitoring functions are available, including supply voltage, cable breaks and overload conditions to provide comprehensive system diagnostics.

The iC-GD is calibrated via SPI and via the relevant pins.

Each IC holds a unique serial number for identification.

PACKAGING INFORMATION QFN38 5 mm x 7 mm to JEDEC Standard

PIN CONFIGURATION QFN38 5 mm x 7 mm



PIN FUNCTIONS

No.	Name	Function
1	ADR0	Address 0 input
2	ADR1	Address 1 input
3	ADR2	Address 2 input
4	VCC	Supply voltage 3.3...5 V
5	GNDL	Logic Ground
6	TEST	Test pin

PIN FUNCTIONS

No.	Name	Function
7	VPD	5 V voltage output
8	VRPH	Modulator mid voltage
9	VREF	Modulator reference voltage
10	LED1	LED1 driver output
11	VNB	Supply voltage -15 V
12	UN1	Voltage negative channel 1
13	UI1	Voltage current channel 1
14	UP1	Voltage positive channel 1
15	IA1	Current output analog/digital channel 1
16	GNDP	Power Ground
17	VDA	Supply voltage 24 V
18	IA2	Current output analog/digital channel 2
19	UP2	Voltage positive channel 2
20	UI2	Voltage current channel 2
21	UN2	Voltage negative channel 1
22	VB	Supply voltage +15 V
23	LED2	LED2 driver output
24	VPA	5 V voltage output
25	RP	Resistor pin 1
26	RN	Resistor pin 2
27	GNDA	Analog Ground
28	NRES	Reset input (low active)
29	RDY	Ready output
30	NCS	Chip select input (low active)
31	SCLK	SPI clock input
32	SDI	SPI data input
33	SDO	SPI data output
34	SYNC1	Synchronization channel 1
35	SYNC2	Synchronization channel 2
36	IRQ	Interrupt output
37	SCL	Serial clock input
38	SDA	Serial data input

The *Thermal Pad* is to be connected to a Ground Plane (GNDP) on the PCB.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VB	Power Supply at VB	Referenced to GNDP	-0.3	18	V
G002	I(VB)	Current in VB		-10	100	mA
G003	VNB	Power Supply at VNB	Referenced to GNDP	-18	0.3	V
G004	I(VNB)	Current in VNB		-10	100	mA
G005	V(VDA)	Voltage at VDA, IA1, IA2	Referenced to the lowest voltage at GNDP, VDA, IA1, IA2; Referenced to the highest voltage of VB, VDA, IA1, IA2	-48	48	V
G006	I(VDA)	Current in VDA		-100	800	mA
G007	V()	Voltage at UP1, UP2, UI1, UI2	Referenced to the lowest voltage of GNDP, VNB, UP1, UP2, UI1, UI2; Referenced to the highest voltage of GNDP, VB, UP1, UP2, UI1, UI2	-48	48	V
G008	V()	Voltage at UN1, UN2	Referenced to GNDP	-48	48	V
G009	V(VCC)	Voltage at VCC	Referenced to GNDL	-0.3	7	V
G010	I(VCC)	Current in VCC		-50	20	mA
G011	I()	Current in IA1, IA2		-800	800	mA
G012	I()	Current in UP1, UP2, UI1, UI2, UN1, UN2		-50	50	mA
G013	V(LED)	Voltage at LED1, LED2	Referenced to GNDP	-0.3	9	V
G014	I(LED)	Current in LED1, LED2		-30	100	mA
G015	V()	Voltage at ADR2, ADR1, ADR0, SCL, SDA, NCS, SCLK, SDI, SDO, NIRQ, NRES, RDY, SYNC1, SYNC2	Referenced to GNDL	-0.3	7	V
G016	I()	Current in ADR2, ADR1, ADR0, NCS, SCLK, SDI, NRES		-4	4	mA
G017	I()	Current in SCL, SDA		-4	120	mA
G018	I()	Current in IRQ, RDY, SYNC1, SYNC2		-25	220	mA
G019	I()	Current in SDO		-260	220	mA
G020	V()	Voltage at VPA, VPD, VREF, VRPH, TEST	Referenced to GNDP	-0.3	7	V
G021	I()	Current in VPA, VPD, VREF, VRPH, TEST		-4	4	mA
G022	V()	Voltage at RP, RN, GNDA	Referenced to GNDP	-0.3	2	V
G023	I()	Current in RP, RN, GNDA, GNDL		-1	1	mA
G024	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G025	Tj,op	Operating Junction Temperature		-40	125	°C
G026	Ts	Storage Temperature		-40	125	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-20		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Surface mounted, thermal pad soldered to approx. 2 cm² heat sink		25	35	K/W
T03	Rthjc	Thermal Resistance Chip/Case			4		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VB	Permissible Supply Voltage	Referenced to GNDP	14.5	15	16	V
002	I(VB)	Supply Current in VB	No load, configuration as digital IO, current output (DI, DO, CO) No load, configuration as voltage/current input (VI, CI) No load, both channels configured as voltage output (VO)	8 12 14	11 16.5 18	14 18 22	mA mA mA
003	VNB	Permissible Supply Voltage	Referenced to GNDP	-16	-15	-14	V
004	I(VNB)	Supply Current in VNB	No load No load, both channels configured as voltage outputs	-10 -16	-5 -10	-2 -4	mA mA
005	VCC	Permissible Supply Voltage	Referenced to GNDL	3.135	3.3	5.25	V
006	I(VCC)	Supply Current in VCC	No load, VCC = 3.3 V No load, VCC = 5 V	2 4	5 9	6 12	mA mA
007	VDA	Permissible Supply Voltage	Referenced to GNDP, VDA not connected to VB	18		36	V
008	VDA	Permissible Supply Voltage	Referenced to GNDP, VDA connected to VB	14.5		16	V
009	I(VDA)	Supply Current in VDA	No load, VDA not connected to VB	0.2	0.6	2	mA
010	I(VDA)	Supply Current in VDA	No load, VDA connected to VB; Configuration as DI, DO, CO Configuration as VI, CI Both channels configured as VO with supply current in VB (Item No. 002)	 9 13 15	 12 16.5 19	 15 19 23	 mA mA mA
011	Vc()lo	Clamp Voltage lo at RP, RN, SCL, SDA, NCS, ADR2, ADR1, ADR0, SCLK, SDI, SDO, IRQ, GNDA, VB, VCC, LED1, LED2, SYNC1, SYNC2, TEST, NRES, RDY, GNDL, VRPH, VREF	vs. GNDP, I() = -10 mA	-1.2		-0.3	V
012	Vc()lo	Clamp Voltage lo at VNB	vs. GNDP, I() = -2 mA	-36		-18	V
013	Vc()lo	Clamp Voltage lo at VDA, IAx, UPx, UIx, UNx	vs. GNDP, I(VDA) = -3 mA, I(IAx) = -12 mA, I(UPx) = -3 mA, I(UIx) = -6 mA, I(UNx) = -3 mA	-60		-46	V
014	Vc()lo	Clamp Voltage lo at VDA	vs. IAx, I() = -5 mA	-60		-46	V
015	Vc()lo	Clamp Voltage lo at VDA, IA1x, UPx, UIx	vs. VB, I(VDA) = -5 mA, I(IAx) = -12 mA, I(UPx, UIx) = -3 mA	-60		-46	V
016	Vc()lo	Clamp Voltage lo at UPx, UIx	vs. VNB, I() = -4 mA	-60		-46	V
017	Vc()hi	Clamp Voltage hi at VNB	vs. GNDP, I() = 2 mA	0.3		1.2	V
018	Vc()hi	Clamp Voltage hi at RP, RN, SCL, SDA, NCS, ADR2, ADR1, ADR0, SCLK, SDI, SDO, IRQ, GNDA, VCC, LED1, LED2, SYNC1, SYNC2, TEST, NRES, RDY, VRPH, VREF	vs. GNDP, I() = 2 mA	6		18	V
019	Vc()hi	Clamp Voltage hi at VB	vs. GNDP, I() = 2 mA	18		36	V
020	Vc()hi	Clamp Voltage hi at VDA, IAx, UPx, UIx, UNx	vs. GNDP; I(VDA) = 5 mA I(IAx) = 15 mA I(UPx) = 4 mA, I(UIx) = 10 mA, I(UNx) = 3 mA Tj = -20 °C	 36 33 46 44		 48 48 60 60	 V V V V
021	Vc()hi	Clamp Voltage hi at VDA	vs. IAx, I() = 2 mA	36		52	V
022	Vc()hi	Clamp Voltage hi at VDA, IA1x, UPx, UIx	vs. GNDP; I(VDA) = 5 mA I(IAx) = 15 mA I(UPx) = 3 mA, I(UIx) = 3 mA, VNB = 0 V Tj = -20 °C	 36 31.5 46 44		 52 48 60 60	 V V V V

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
023	Vc()hi	Clamp Voltage hi at UPx, UIx	vs. VNB, I() = 3 mA Tj = -20 °C	46 44		60 60	V V
024	Ipu()	Pull-up Current from SCL, SDA, NCS, ADR2, ADR1, ADR0, SYNC1, SYNC2, NRES, RDY, SCLK, SDI	V() = 0.8 * VCC	-100		-10	µA
025	Ipu()	Pull-up Current from SCL, SDA, NCS, ADR2, ADR1, ADR0, SYNC1, SYNC2, NRES, RDY, SCLK, SDI	V() = 0 V	-220		-20	µA
026	Vt()hi	Threshold Voltage hi at inputs SCLK, SDI, NRES, SCL, SDA, NCS, ADR2, ADR1, ADR0, SYNC1, SYNC2				2	V
027	Vt()lo	Threshold Voltage lo at inputs SCLK, SDI, NRES, SCL, SDA, NCS, ADR2, ADR1, ADR0, SYNC1, SYNC2		0.8			V
028	Vt()hys	Hysteresis at inputs SCLK, SDI, NRES, RDY, SCL, SDA, NCS, ADR2, ADR1, ADR0, SYNC1, SYNC2		100	200	400	mV
029	Vs()lo	Saturation Voltage lo at outputs SDO, NIRQ, SYNC1, SYNC2, RDY	I() = 8 mA, SDO = NIRQ = SYNC1 = SYNC2 = RDY = lo			0.4	V
030	Vs()lo	Saturation Voltage lo at outputs SCL, SDA	I() = 4 mA, SCL = SDA = lo			0.4	V
031	Vs()hi	Saturation Voltage hi at output SDO	Vs() = VCC − V(), I() = -8 mA, SDO = hi			0.4	V
032	Isc()lo	Short-Circuit Current lo in outputs SDO, IRQ, SYNC1, SYNC2, RDY	V() = VCC, SDO = IRQ = SYNC1 = SYNC2 = RDY = lo	20		200	mA
033	Isc()lo	Short-Circuit Current lo in outputs SCL, SDA	V() = VCC, SCL = SDA = lo	10		100	mA
034	Isc()hi	Short-Circuit Current hi from output SDO	V() = 0V, SDO = hi	-250		-25	mA
035	tRESlo	Minimum Time lo at NRES		300			ns
Bias							
201	V(RP)	Voltage at RP	RREF = 20 kΩ ± 0.1% vs. RN, ATK(7:0) = 0x80	1.1	1.185	1.28	V
202	V(RP)ab	Calibration Accuracy of voltage at RP	RREF = 20 kΩ ± 0.1% vs. RN	-0.06		0.06	%
203	V(RP),TK	Temperature Dependency of voltage at RP	RREF = 20 kΩ ± 0.1% vs. RN, bandgap calibrated	-0.065		0.065	%
204	Isc,max()	Short-Circuit Current lo in RP	V(RP) = 0 V	100	250	500	µA
Oscillator							
301	fos	Oscillator Frequency	Initial, not calibrated	1.6	2	2.5	MHz
302	fos,PLL	Oscillator Frequency PLL	Initial, not calibrated	12.8	16	20	MHz
303	fos	Calibration Accuracy of oscillator frequency	fos_{nom} = 16 MHz	-1.5		1.5	%
304	fos,TK	Temperature Dependency of oscillator frequency	fos_{nom} = 16 MHz	-3		3	%
305	V(pll,fos)	Clock Divider Ratio			8		

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Interface							
501	fscl	Maximum Permissible Clock Frequency I2C				100	kHz
502	fclk	Maximum Permissible Clock Frequency SPI	Internal oscillator calibrated	12.5			MHz
503	fclk_na	Maximum Permissible Clock Frequency SPI	Internal oscillator not calibrated	6.0			MHz
504	tCL	Minimum Time SCLK low	Low defined by TTL threshold Vt()lo	32.5			ns
505	tCH	Minimum Time SCLK high	High defined by TTL threshold Vt()hi	22			ns
506	tSU	Setup Time: SDI valid before SCLK → low	Validity defined by Vt()lo or Vt()hi	3			ns
507	tH	Hold Time: SDI valid to SCLK → low	Validity defined by Vt()lo or Vt()hi	15			ns
508	tPOmin	Output Delay SDO → valid to SCLK → high	Validity defined by Vs()lo or Vs()hi, CL(SDO) ≤ 30 pF	0			ns
509	tPOmax	Output Delay SDO → valid to SCLK → high	Validity defined by Vs()lo or Vs()hi, CL(SDO) ≤ 30 pF			30	ns
510	tPOT	Output Delay SDO → tri-state to NCS → high				50	ns
511	tCSU	Setup Time: NCS → low before SCLK → low	Internal oscillator calibrated	50			ns
512	tCSU_na	Setup-Time: NCS → low before SCLK → low	Internal oscillator not calibrated	75			ns
513	tCSH	Hold Time: NCS → high to SCLK → high	Internal oscillator calibrated	200			ns
514	tCSH_na	Hold Time: NCS → high to SCLK → high	Internal oscillator not calibrated	300			ns
515	tD	Minimum Time NCS high	hi defined by TTL threshold Vt()hi, internal oscillator calibrated	100			ns
516	tD_na	Minimum Time NCS high	hi defined by TTL threshold Vt()hi, internal oscillator not calibrated	150			ns
5 V Regulator VPA, VPD							
601	V(VPA)	Voltage at VPA	CVPA = 100 nF, bandgap calibrated	5	5.25	5.5	V
602	Isc(VPA)	Short-Circuit Current from VPA	VPA = 0 V	-100		-10	mA
603	VtUlo	Lower Undervoltage Threshold VPA		3.5	4		V
604	VtUhi	Upper Undervoltage Threshold VPA			4.4	4.75	V
605	VtUhys	Hysteresis Undervoltage VPA		200	400	800	mV
606	V(VPD)	Voltage at VPD	CVPD = 100 nF, bandgap calibrated	5	5.25	5.5	V
607	Isc(VPD)	Short-Circuit Current from VPD	VPD = 0 V	-120		-15	mA
608	VtUlo	Lower Undervoltage Threshold VPD		3.3	3.8		V
609	VtUhi	Upper Undervoltage Threshold VPD			4.2	4.6	V
610	VtHys	Hysteresis Undervoltage VPD		200	400	800	mV
Voltage Monitor VB, VNB, VCC, VDA							
701	Vt(VB)lo	Lower Undervoltage Threshold VB		12.6	13.3		V
702	Vt(VB)hi	Upper Undervoltage Threshold VB			13.9	14.4	V
703	V(VB)hys	Hysteresis Undervoltage VB	VBhys = Vt(VB)hi − Vt(VB)lo	200	500	800	mV
704	Vt(VNB)lo	Upper Undervoltage Threshold VNB			-13	-12.3	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
705	Vt(VNB)hi	Lower Undervoltage Threshold VNB		-13.9	-13.5		V
706	V(VNB)hys	Hysteresis Undervoltage VNB	VNBhys = Vt(VNB)hi − Vt(VNB)lo	-800	-500	-200	mV
707	Vt(VCC)lo	Lower Undervoltage Threshold VCC		2.8	2.9		V
708	Vt(VCC)hi	Upper Undervoltage Threshold VCC			3	3.13	V
709	V(VCC)hys	Hysteresis Undervoltage VCC	VCChys = Vt(VCC)hi − Vt(VCC)lo	50	100	300	mV
710	Vt(VDA)lo	Lower Undervoltage Threshold VDA	Bit VDA_VB = lo	15	16		V
711	Vt(VDA)hi	Upper Undervoltage Threshold VDA	Bit VDA_VB = lo		16.5	17.5	V
712	V(VDA)hys	Hysteresis Undervoltage VDA	VDAhys = Vt(VDA)hi − Vt(VDA)lo, bit VDA_VB = lo	250	500	1000	mV
713	ΔV(VB,VDA)	Error Message at voltage difference between VB and VDA	ΔV(VB,VDA) = MAX(|VB − VDA|), bit VDA_VB = hi	0.75			V
Temperature Monitor							
901	T1off	Thermal Shutdown Temperature	Increasing temperature Tj	125	140	155	°C
902	T1on	Thermal Shutdown Reset Temperature	Decreasing temperature Tj	115	130	145	°C
903	T1hys	Thermal Hysteresis 1	T1hys = T1off − T1on	5	10	20	°C
904	T2off	Thermal Shutdown Temperature 2	Increasing temperature Tj	145	160	175	°C
905	T2on	Thermal Shutdown Reset Temperature 2	Decreasing temperature Tj	135	150	165	°C
906	T2hys	Thermal Hysteresis 2	T2hys = T2off − T2on	5	10	25	°C
907	dToff	Difference Thermal Shutdown Temperature	dToff = T2off − T1off	10	20	40	°C
908	dTon	Difference Thermal Shutdown Reset Temperature	dTon = T2on − T1on	10	20	40	°C
909	R()	Temperature Converter Resolution	Range -64...191 °C	8			Bit
910	R()	Temperature Converter Range	Minimum usable temperature range	-41		183	°C
911	Toffset	Maximum Temperature Offset	Calibration via AOCT(4:0)	-16		15	LSB
912	Tdiff()	Temperature Converter Difference	After calibration; Tj = 25 °C Tj = -20...105 °C	 -1 -2		 1 2	 °C °C
Digital Outputs IAx, x = 1, 2							
B01	Vs()hi	Saturation Voltage hi at IAx	Vs(IAx)hi = VDA − V(), I(IAx) = -200 mA, T < T2on; -20 °C 27 °C 105 °C			 0.5 0.7 0.9	 V V V
B02	Vs()hi	Saturation Voltage hi at IAx	Vs(IAx)hi = VDA − V(), I(IAx) = -500 mA, high-side driver active, T < T2on			2	V
B03	Isc()hi	Short-Circuit Current hi from IAx	VDA − 36 V < V(IAx) < VDA − 3 V, high-side driver active, T < T1on	-800		-505	mA
B04	Ipu()	Pull-up Current	Hi-side driver configuration, IAx = lo, VDA = 18...32 V; V() = VDA − 2 V...VB V() = VB...VB − 3 V V() = VB −3 V...0 V	 -100 -120 -120		 -10 -40 -80	 µA µA µA
B05	Vpu()	Pull-up Voltage	Vpu() = V() − VDA, I() = -5...5 µA, hi-side driver configuration, IAx = lo, pull-up current active	-1.8			V
B06	Vto()hi	Upper Trigger Threshold hi at IAx	Vto() = VDA − V(IAx)	2.2	2.45	2.9	V
B07	Vtu()hi	Lower Trigger Threshold hi at IAx	Vtu() = VDA − V(IAx)	2.3	2.7	3	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B08	Vhys()hi	Hysteresis Trigger Threshold hi at IAx	Vhys,hi = Vto()hi − Vtu()hi	100	250	600	mV
B09	Vs()lo	Saturation Voltage lo at IAx	I(IAx) = 200 mA, low-side driver active, T < T2on; Tj = -20 °C Tj = 25 °C Tj = 105 °C			 0.6 0.8 0.94	 V V V
B10	Vs()lo	Saturation Voltage lo at IAx	I(IAx) = 500 mA, low-side driver active, T < T2on			2.35	V
B11	Isc()lo	Short-Circuit Current lo from IAx	3 V < V(IAx) < 36 V, low-side driver active, T < T1on	505		800	mA
B12	Ipd()	Pull-down Current	Lo-side driver configuration, IAx = hi, VDA = 18...32 V V() = 2 V...VB − 3 V, V(LED) < 3 V V() = VB − 3 V...VB, V() = VB...VDA	 15 15 30	 20	 25 80 160	 µA µA µA
B13	Vpd()	Pull-down Voltage	I() = -5...5 µA, lo-side driver configuration, IAx = hi, pull-down current active			1	V
B14	Vs()lo,r	Saturation Voltage lo at IAx	I(IAx) = -200 mA, low-side driver active, T < T2on	-1.2	-0.6	0	V
B15	Ir,max()	Maximum Reverse Current from IAx	-2 V < V() < GNDP, low-side driver active VB − 36 V < V() < -2 V	-800 -10		0 0	mA mA
B16	Vto()lo	Upper Trigger Threshold lo at IAx	ENDOSC_x = lo	2.35	2.7	3	V
B17	Vtu()lo	Lower Trigger Threshold lo at IAx	ENDOSC_x = lo	2.2	2.5	2.9	V
B18	Vhys()lo	Hysteresis Trigger Threshold lo at IAx	ENDOSC_x = lo, Vhys,lo = Vto()lo − Vtu()lo	100	300	500	mV
B19	Ilk()	Leakage Current in IAx	Output, pull-up, pull-down current inactive; V(IAx) = 0 V...VB − 3 V V(IAx) = VB − 3 V...VDA	 -1 -1		 1 120	 µA µA
B20	Ir()	Reverse Current in IAx	V(IAx) > VDA + 0.1 V	0		2	mA
B21	f()max,out	Maximum Output Frequency	Digital output as output	125			kHz
B22	f()max,in	Maximum Input Frequency	Digital output as input	125			kHz
B23	td(),ol	Delay to open-load detection		1		2	ms
B24	Vf()hi	Free-Wheeling Voltage hi at IAx	Low-side driver configuration, vs. GND, I(IAx) = 80 mA, IAx = hi, L = 10 mH	36	41	48	V
B25	Vf()lo	Free-Wheeling Voltage lo at IAx	High-side driver configuration, vs. VDA, I(IAx) = -80 mA, IAx = lo, L = 10 mH	-54	-44	-40	V
B26	tr	Rise Time	IAx: 3 V → 13 V			869	ns
B27	tf	Fall time	IAx: VDA − 3 V → 8 V, VDA = 18...30 V			869	ns
B28	Vto()lo	Upper Threshold lo at IAx	ENDOSC_x = hi	1	1.3	1.6	V
B29	Vtu()lo	Lower Threshold lo at IAx	ENDOSC_x = hi	0.8	1	1.4	V
B30	Vhys()lo	Hysteresis Threshold lo at IAx	ENDOSC_x = hi, Vhys,lo = Vto()lo − Vtu()lo	100	300	500	mV
Digital Inputs IAx, x = 1, 2							
C01	Vt()hi	Upper Input Threshold			10	11	V
C02	Vt()lo	Lower Input Threshold		5	8		V
C03	Vhys()	Hysteresis at IAx	Vhys() = Vt()hi − Vt()lo	1	2	3	V
C04	Ipu()	Pull-up Current	V() = VDA − 3... 0 V, DI_SEL_x = 00 VDA = 18...32 V VDA = 18...36 V	 -6 -6	 -3 -3	 -2 -1	 mA mA
C05	Vpu()	Pull-up Voltage	Vpu() = V() − VDA, I() = -1 mA, DI_SEL_x = 00	-2.5			V

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C06	Ipd()	Pull-down Current	Type 1, V() > 15...30 V, DI_SEL_x = 01 Type 1, V() > 30...36 V, DI_SEL_x = 01 Type 2, V() > 11...30 V, DI_SEL_x = 10 Type 2, V() > 30...36 V, DI_SEL_x = 10 Type 3, V() > 11...30 V, DI_SEL_x = 11, default (after startup) Type 3, V() > 30...36 V, DI_SEL_x = 11, default (after startup)	0.2 0.4 4 4 0.2 0.4		1 6 6 8 1 6	mA mA mA mA mA mA
C07	Ipd()	Pull-down Current	Type 1, V() > 15..30 V, DI_SEL_x = 01 Type 1, V() > 30...36 V, DI_SEL_x = 01 Type 2, V() > 11...30 V, DI_SEL_x = 10 Type 2, V() > 30...36 V, DI_SEL_x = 10 Type 3, V() > 11...30 V, DI_SEL_x = 11, default (after startup) Type 3, V() > 30...36 V, DI_SEL_x = 11, default (after startup), external LED connected at Pin LED to GND or Pin LED connected to GND	2 2 6 6 2 2	2.8 7 2.8 	6 8 10 12 6 8	mA mA mA mA mA mA
C08	Ipd()	Pull-down Current	Type 1, V() = 5..15 V, DI_SEL_x = 01 Type 2, V() = 5..11 V, DI_SEL_x = 10 Type 3, V() = 5..11 V, DI_SEL_x = 11, default (after startup)	1.5 5 1.5		6 10 6	mA mA mA
C09	Vpd()	Pull-down Voltage	Type 1..3, I() = 100 µA, DI_SEL_x = 01, 10, 11			3	V
C10	Ipd()	Pull-down Current	V() = 5...11 V, no supply voltage VDA V() > 11...30 V, no supply voltage VDA V() > 30..36 V, no supply voltage VDA additionally Item No. E05 applies, if an LED at pin LED vs. GNDP is connected or pin LED is connected to GNDP	2 2 2		15 8 10	mA mA mA
C11	f()max	Maximum Input Frequency		150			kHz
LED Output LEDx x = 1, 2							
E01	Vo()lo	Open-loop Voltage lo at LEDx	Digital input: V(IAx) < 5 V, digital output: V(IAx) < 2.2 V	0		0.2	V
E02	Vo()hi	Open-loop Voltage hi at LEDx	Digital input: V(IAx) < 11 V, digital output: V(IAx) > VDA − 2.2 V	3.5		8.5	V
E03	Vs()lo	Saturation Voltage lo at LEDx	I(LEDx) = 5 mA, digital input: V(IAx) = 0...5 V, digital output: V(IAx) = 0...2.2 V	0	0.2	0.4	V
E04	Isc()hi	Short-Circuit Current hi from LEDx	0 V < V(LEDx) < 3 V, type 1..3 or pull-up current selected by DI_SEL_x, digital input: V(IAx) > 11 V, digital output: V(IAx) > VDA − 2.2 V	-4	-2.5	-2	mA
E05	Isc()hi	Short-Circuit Current hi from LEDx	No supply voltage, digital input: 0 V < V(LEDx) < 3 V, V(IAx) > 11 V	-7	-3.5	-1.8	mA
E06	Isc()lo	Short-Circuit Current lo in LEDx	V(LEDx) = 0.5...4 V, digital input: V(IAx) = 0...5 V, digital output: V(IAx) = 0...2.2 V	10		100	mA
Analog Outputs IAx, UPx, UNx, UIx, x = 1, 2							
I01	Vo()	Voltage-Output Range at UPx, UNx	Voltage output configuration, I(UPx) = ±10 mA or -20...10 mA in extended current mode (VO_EC_x = 1), after calibration	-10.5		10.499	V
I02	Io(UPx)hi	Short-Circuit Current hi	Voltage output configuration, UPx = VNB	-16	-13	-10.5	mA
I03	Io(UPx)hi	Short-Circuit Current hi	Voltage output configuration, UPx = VNB, extended current range (VO_EC_x = 1)	-30	-25	-21	mA
I04	Io(UPx)lo	Short-Circuit Current lo	Voltage output configuration, UPx = VB	10.5	13	16	mA
I05	Vs(UNx)lo	Saturation Voltage lo at UNx	I(UNx) = 21.5 mA	0	0.9	1.5	V
I06	Vs(UNx)lo	Saturation Voltage lo at UNx	I(UNx) = -21.5 mA	-1.5	-0.8	0	V
I07	Isc(UNx)lo	Short-Circuit Current in UNx	vs. GNDP, V(UNx) = 2...40 V, T < Toff2	22	28	35	mA
I08	Isc(UNx)lo	Short-Circuit Current in UNx	vs. GNDP, V(UNx) = -40...-2 V, T < Toff2	-100	-40	-22	mA

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I09	Isc(UNx)lo	Short-Circuit Current from UNx	vs. GNDP, V(UNx) = -40...-2 V, T > Toff2	-50		-1	mA
I10	Ior(IAx)	Current-Output Range	Range 1, current output configuration, V(IAx) = 0...12 V, after calibration	0		20.999	mA
I11	Ior(IAx)	Current-Output Range	Range 2, current output configuration, V(IAx) = 0...12 V, after calibration	4		20.999	mA
I12	Ior(IAx)	Current-Output Range	Range 3, current output configuration, V(IAx) = 0...12 V, after calibration	0		2.0999	mA
I13	Ior(IAx)	Current-Output Range	Range 4, current output configuration, V(IAx) = 0...12 V, after calibration	0		209.99	µA
I14	Io(IAx)	Output Current	PT100 measurement, VDA = 24 V ±1 V, V(IAx) = 0.1...0.64 V, after calibration Tj = -40 °C Tj = 25 °C Tj = 100 °C Tj = 120 °C	 1.6975 1.6995 1.6975 1.6925	 1.7 	 1.7025 1.7005 1.7025 1.7075	 mA mA mA mA
I15	Io(IAx)	Output Current	PT1000 measurement, VDA = 24 V ±1 V, V(IAx) = 0.1...0.64 V, after calibration Tj = -40°C Tj = 25°C Tj = 100°C Tj = 120°C	 169.75 169.95 169.75 169.25	 170 	 170.25 170.05 170.25 170.75	 µA µA µA µA
I16	Ir(IAx,UIx)	Output Current-Ratio	PT 3-wire measurement, V(IAx) − V(UIx) = 0...1 V	0.99	1	1.02	
I17	Ilor(IAx)	Load Regulation	Output current range 1 to 3, V() = 0...10 V Output current range 4, V() = 0...10 V Output current range 4, V() = 0.1...0.64 V	-0.1 -0.15 -0.1		0.1 0.15 0.1	%FS %FS %FS
I18	Vto()hi	Upper Trigger Threshold hi at IAx, UIx	Current output configuration, Vto()hi = VB − V(IAx), three-terminal mode: Vto()hi = VB − V(UIx)	1.6	1.9	2.2	V
I19	Vtu()hi	Lower Trigger Threshold hi at IAx, UIx	Current output configuration, Vtu()hi = VB − V(IAx), three-terminal mode: Vto()hi = VB − V(UIx)	1.8	2.2	2.6	V
I20	Vhys()hi	Hysteresis Trigger Threshold hi at IAx, UIx	Vhys,hi = Vto()hi − Vtu()hi	100	300	600	mV
I21	C	Permissible Capacitor at IAx, UPx, UIx, UNx	Voltage output configuration			1	µF
I22	L	Permissible Inductor at IAx, UIx	Current output configuration			10	mH
VRP Reference Voltage							
J01	V(VRP)ab	Calibration Accuracy of Voltage Reference VRP	vs. VRN, VRPnom = 5.25 V	-0.02		0.02	%
J02	Ioff	Calibration Accuracy of Current Output (offset, 4 mA)	Bandgap calibrated, RREF = 20 kΩ ±0.1%, Inom = 4 mA	-0.05		0.05	%
J03	Igain	Calibration Accuracy of Current Output (gain, 21 mA)	Bandgap calibrated, RREF = 20 kΩ ±0.1%, Inom = 21 mA	-0.05		0.05	%
Analog Inputs UPx, UNx, UIx, x = 1, 2							
M01	Vm()U1	Permissible Voltage Range	Measurement range 1, after calibration	-10.5		10.499	V
M02	Vm()U2	Permissible Voltage Range	Measurement range 2, after calibration	-1.05		1.0499	V
M03	Vm()U3	Permissible Voltage Range	Measurement range 3, after calibration	-105		104.99	mV
M04	Vm()U4	Permissible Voltage Range	Measurement range 4, after calibration	-10.5		10.499	mV
M05	Vm()U5	Permissible Voltage Range	Measurement range 5, after calibration	-17.5		87.5	mV
M06	Vm()U6	Permissible Voltage Range	Measurement range 6, after calibration	-4.375		21.875	mV
M07	Vm()I1	Permissible Current Range	Measurement range 1, after calibration	-21		20.999	mA
M08	Vm()I2	Permissible Current Range	Measurement range 2, after calibration	-13		20.999	mA
M09	Ri()U	Input Resistor between UP1 and UI1 or UP2 and UI2	Voltage input configuration	10	15	20	MΩ

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
M10	Ri()	Input Resistance between UPx and UIx	Current input configuration	200	250	300	Ω
M11	Rm()I	Input Resistance between UP1 and UI1 or UP2 and UI2	Current input configuration, measurement range 1	115	144	175	Ω
M12	Rm()I	Input Resistance between UP1 and UI1 or UP2 and UI2	Current input configuration, measurement range 2	140	178	215	Ω
M13	Imax()	Input Current limitation	Current input configuration; positive, in UPx negative, from UPx	 25 -80	 35 -55	 50 -30	 mA mA
M14	Ipu(UPx)	Pull-Up Current from UPx	V() = VNB...VNB + 3 V V() = VNB + 3 V...VB − 1.5 V V() = VB − 1.5 V...VB	-200 -1 -1	 -0.7	-0.33 -0.33 0	µA µA µA
M15	Ipd(UIx)	Pull-Down Current in UIx	ENVIF_x = lo, voltage measurement, V() = -4...4 V, V() = -4 V...VB − 3 V	0.15	0.3	0.5	µA
M16	dI()	Difference Pull-up/Pull-down current	ENVIF_x = lo, current measurement, I() = |Ipu(UPx)| − Ipd(UIx), V(UPx) = V(UIx) = VNB + 3 V...VB − 3 V	0.1	0.4	0.8	µA
M17	Irev(UPx),n	Current from UPx	V() = VB − 46 V...VNB, V(UIx) = 0 V	-10		0	mA
M18	Irev(UPx),p	Current in UPx	V() = VB...VNB + 46 V	0		2	mA
M19	Irev(UIx),p	Current in UIx	ENVIF_x = lo; V() = VB − 3 V...VB, V(UPx) = 0 V V() = VB...VNB + 46 V, V(UPx) = 0 V	 0.15 1		 100 2000	 µA µA
M20	Irev(UIx),n	Current from UIx	ENVIF_x = lo, V() = VB − 46 V... 4 V	-10000		+0.5	µA
M21	Vto(UPx)	Upper Threshold at UPx	Voltage/current measurement configuration, Vto(UPx) = VB − V(UPx)	0.8	1.3	1.8	V
M22	Vtu(UPx)	Lower Threshold at UPx	Voltage/current measurement configuration, Vtu(UPx) = VB − V(UPx)	0.9	1.4	1.9	V
M23	Vhys(UPx)	Hysteresis Threshold at UPx	Vhys(UPx) = Vto(UPx) − Vtu(UPx)	40	150	400	mV
M24	Vto(UIx)	Upper Threshold at UIx	Voltage measurement configuration	-5	-4.3	-3.6	V
M25	Vtu(UIx)	Lower Threshold at UIx	Voltage measurement configuration	-5.1	-4.4	-3.7	V
M26	Vhys(UIx)	Hysteresis Threshold at UIx	Voltage measurement configuration	40	150	400	mV
M27	Vto(UIx)	Upper Threshold at UIx	Current measurement configuration, Vto(UIx) = V(UIx) − VNB	0.8	1.3	1.8	V
M28	Vtu(UIx)	Lower Threshold at UIx	Current measurement configuration, Vtu(UIx) = V(UIx) − VNB	0.9	1.4	1.9	V
M29	Vhys(UIx)	Hysteresis Threshold at UIx	Current measurement configuration, Vhys(UIx) = Vto(UIx) − Vtu(UIx)	40	150	400	mV
M30	Vgl()U	Common-Mode Range	Voltage measurement (range 1, 2)	-1		1	V
M31	Vgl()	Common-Mode Range	Voltage measurement (range 3)	-1		4	V
M32	Vgl()	Common-Mode Range	Voltage measurement (range 4...6)	-3		3	V
M33	Vgl()I	Common-Mode Range	Current measurement	-6		6	V
M34	R(UIx)	Input Resistance at UIx	ENVIF_x = hi; V(UIx) = VNB...0 V V(UIx) = 0...1 V	 20k 20k		 50k 100k	 kΩ kΩ
M35	Ipd(UIx)	Pull-Down Current at UIx	ENVIF_x = hi, V(UIx) = 1 V... VB	15		200	µA
SAR A/D-Converter							
N01	R()	Resolution SAR-Converter		14			Bit
N02	Offerr()	Offset-Error Voltage Measurement	Measurement referenced to pin RN	-0.5		0.5	%FS
N03	Offerr()	Offset-Error Current-Measurement Digital Output Hi-Side or Lo-Side driver	Tj = 25 °C Tj = -20...100 °C Tj = -20...120 °C	-1 -2 -3	0.2	1 2 3	%FS %FS %FS
N04	Verr()	Gain-Error Voltage Measurement	Measurement Range 0...2.625 V, referenced to pin RN	-4		4	%FS

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N05	Verr()	Gain-Error Current-Measurement Digital Output Hi-Side or Lo-Side driver	Measurement Range |0...200 mA|, %FS ≙ 200 mA	-10		10	%FS
N06	Verr()	Gain-Error Current-Measurement Digital Output Hi-Side or Lo-Side driver	Measurement Range |200...500 mA|, %FS ≙ 500 mA	-10		10	%FS
N07	Tct	Conversion Rate	One channel Two channels Three channels Four channels Five channels All analog channels count (inputs, outputs, PT-elements count double) as well as diagnostics measurement	30 15 10 7.5 6			kHz kHz kHz kHz kHz
D/A-Converter							
O01	R()	Resolution		14			Bit
O02	Offerr()U	Offset-Error Voltage Output	Tj = 25 °C, input: 0x0000 Tj = -20...100 °C, input: 0x0000 Tj = -20...120 °C, input: 0x0000	-0.015 -0.03 -0.06		0.015 0.03 0.06	%FS %FS %FS
O03	Tc()off	Temperature-Coefficient Offset-Error	Tj = 100...120 °C, referenced to 100 °C, input: 0x0000	-0.0015		0.0015	%FS/°C
O04	Gainerr()U	Gain-Error Voltage Output	Tj = 25 °C, input: 0xE000, 0x1FFF Tj = -20...100 °C, input: 0xE000, 0x1FFF Tj = -20...120 °C, input: 0xE000, 0x1FFF	-0.025 -0.07 -0.14		0.025 0.07 0.14	%FS %FS %FS
O05	Tc()gain	Temperature-Coefficient Gain-Error	Tj = 100...120 °C, referenced to 100 °C, input: 0xE000, 0x1FFF	-0.0035		0.0035	%FS/°C
O06	Offerr()I	Offset-Error Current Output	Range 1...3, Tj = 25 °C, input: 0x0000 Range 1...3, Tj = -20...100 °C, input: 0x0000 Range 1...3, Tj = -20...120 °C, input: 0x0000 Range 4, Tj = 25 °C, input: 0x0000 Range 4, Tj = -20...100 °C, input: 0x0000 Range 4 Tj = -20...120 °C, input: 0x0000	-0.06 -0.12 -0.24 0 0 0		0.06 0.12 0.24 0.6 0.6 1.0	%FS %FS %FS %FS %FS %FS
O07	Tc()off	Temperature-Coefficient Offset-Error Current Output	Range 1...3, Tj = 100...120 °C, referenced to 100 °C, input: 0x0000 Range 4, Tj = 100...120 °C, referenced to 100 °C, Eingang: 0x0000	-0.006 0		0.006 0.02	%FS/°C %FS/°C
O08	Gainerr()I	Gain-Error Current Output	Range 1...3, Tj = 25 °C, input: 0x3FFF Range 1...3, Tj = -20...100 °C, input: 0x3FFF Range 1...3, Tj = -20...120 °C, input: 0x3FFF Range 4, Tj = 25 °C, input: 0x3FFF Range 4, Tj = -20...100 °C, input: 0x3FFF Range 4, Tj = -20...120 °C, input: 0x3FFF	-0.14 -0.28 -0.56 -0.6 -0.6 -1.0		0.14 0.28 0.56 0 0 0	%FS %FS %FS %FS %FS %FS
O09	Tc()gain	Temperature-Coefficient Gain-Error Current Output	Range 1...3, Tj = 100...120 °C, referenced to 100 °C, input: 0x3FFF Range 4, Tj = 100...120 °C, referenced 100 °C, input: 0x3FFF	-0.014 -0.02		0.014 0	%FS/°C %FS/°C
O10	DNL	Differential Nonlinearity		-0.25		0.25	LSB
O11	Tcr	Conversion Rate	One channel Two channels Three channels Four channels Five channels All analog channels count (inputs, outputs, PT-elements count double) as well as diagnostics measurement	30 15 10 7.5 6			kHz kHz kHz kHz kHz
O12	Tov()U	Overshoot		-2		2	%FS
O13	Tov()I			-1		1	%FS
O14	Tsu	Settling Time	to > 99% full-scale			20	µs

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ΔΣ A/D-Wandler							
S01	R()	Resolution		14			Bit
S02	Err()U	Voltage-Measurement Error	Tj = 25 °C Tj = -20...100 °C Tj = -20...120 °C	-0.05 -0.15 -0.2		0.05 0.15 0.2	%FS %FS %FS
S03	Tc()off	Voltage-Measurement Temperature-Coefficient Error	Tj = 100...120 °C, referenced to 100 °C	-0.0025		0.0025	%FS/°C
S04	CMerr()U	Voltage-Mesurement Common-Mode Error	Range 1 Range 2 Range 3 Range 4 Range 5 Range 6	-0.04 -0.08 -0.20 -0.25 -0.20 -0.20	0 0 0 0 0 0	0.04 0.08 0.20 0.25 0.20 0.20	%FS/V %FS/V %FS/V %FS/V %FS/V %FS/V
S05	Err()I1	Current-Measurement Error	Range 1, Tj = 25 °C Range 1, Tj = -20...100 °C Range 1, Tj = -20...120 °C Range 2, Tj = 25 °C Range 2, Tj = -20...100 °C Range 2, Tj = -20...120 °C	-0.1 -0.2 -0.3 -0.2 -0.4 -0.6		0.1 0.2 0.3 0.2 0.4 0.6	%FS %FS %FS %FS %FS %FS
S06	Tc()off	Current-Measurement Temperature-Coefficient Error	Range 1, Tj = 100...120 °C, referenced to 100 °C Range 2, Tj = 100...120 °C, referenced to 100 °C	-0.005 -0.01		0.005 0.01	%FS/°C %FS/°C
S07	CMerr()I	Current-Measurement Common-Mode Error	Range 1 Range 2	-0.08 -0.16	0 0	0.08 0.16	%FS/V %FS/V
S08	Err()T	Temperature-Mesurement Error	Type J, K, N, E, PTxxx, Tj = 25 °C Type J, K, N, E, PTxxx, Tj = -20...100 °C Type J, K, N, E, PTxxx, Tj = -20...120 °C Type R, S, B, Tj = 25 °C Type R, S, B, Tj = -20...100 °C Type R, S, B, Tj = -20...120 °C Type T, Tj = 25 °C Type T, Tj = -20...100 °C Type T, Tj = -20...120 °C	-0.15 -0.3 -0.5 -0.2 -0.4 -0.7 -0.3 -0.6 -1.2		0.15 0.3 0.5 0.2 0.4 0.7 0.3 0.6 1.2	%FS %FS %FS %FS %FS %FS %FS %FS %FS
S09	Tc()	Temperature-Coefficient Temperature-Mesurement Error	Type J, K, N, E, PTxxx Tj = 100...120 °C, referenced to 100 °C Type R, S, B, Tj = 100...120 °C, referenced to 100 °C Type T, Tj = 100...120 °C, referenced to 100 °C	-0.01 -0.015 -0.03		0.01 0.015 0.03	%FS/°C %FS/°C %FS/°C
S10	CMerr()T	Thermo-Couples Common-Mode Error	Range J Range K Range T Range N Range E Range R Range S Range B	-0.36 -0.43 -1.38 -0.64 -0.39 -0.65 -0.62 -0.68	0 0 0 0 0 0 0 0	0.36 0.43 1.38 0.64 0.39 0.65 0.62 0.68	%FS/V %FS/V %FS/V %FS/V %FS/V %FS/V %FS/V %FS/V
S11	FIL	Filter Settings	Maximum cut-off frequency for achieving the stated accuracy (variance of measured values significantly smaller than permissible measurement error at Tj = 25 °C) ±10 V, ±1 V, ±100 mV, ±20 mA, 4...20 mA, PTxxx -17.5...87.5 mV, TE JKTNE ±10 mV -4.375...21.875 mV, TE RSB			arbitrary 1000 250 125	Hz Hz Hz Hz
S12	DNL	Differential Nonlinearity		-1		1	LSB
S13	INL	Integrale Nonlinearity		-1		1	LSB
S14	Tov	Overshoot		-1		1	%FS
S15	V(VRPH)	Voltage at VRPH		2.5	2.625	2.75	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VB = 14.5...16 V, VNB = -15 V ±1 V, VDA = 18...36 V or VDA = VB, VCC = 3.3...5 V ±5%, RREF = 20 kΩ ±0.1% TK5, Tj = -20...105 °C, if not otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
S16	Isc()hi	Short-Circuit Current hi from VRPH	V(VRPH) = 0 V	-20	-6.5	-2	mA
S17	Isc()lo	Short-Circuit Current lo from VRPH	V(VRPH) = 5 V	5	17.5	40	mA
S18	V(VREF)	Voltage at VREF	VREF = VRPH − 1.33 ∗ VBG	0.8	1	1.2	V
S19	Isc()hi	Short-Circuit Current hi from VREF	V(VREF) = 0 V	-30	-7.5	-3	mA
S20	Isc()lo	Short-Circuit Current lo from VREF	V(VREF) = 5 V	3	12.5	30	mA
Startup Behaviour							
T01	tir	Maximum Start-up-Time normal mode	NCS at '1' during self-configuration phase (from 30 µs to poweron/reset, until RDY at '1')		40	80	ms
T02	tif	Maximum Start-up-Time fast mode: EEPROM data will be not read	NCS at '0', SCLK at '1' during self-configuration phase (from 30 µs to poweron/reset, until RDY at '1')		0.5		ms
T03	tix	Maximum Start-up-Time ultra fast mode: EEPROM and zapping data will be not read	NCS at '0', SCLK at '0' during self-configuration phase (from 30 µs to poweron/reset, until RDY at '1')		0.08		ms

EXTERNAL CIRCUITRY

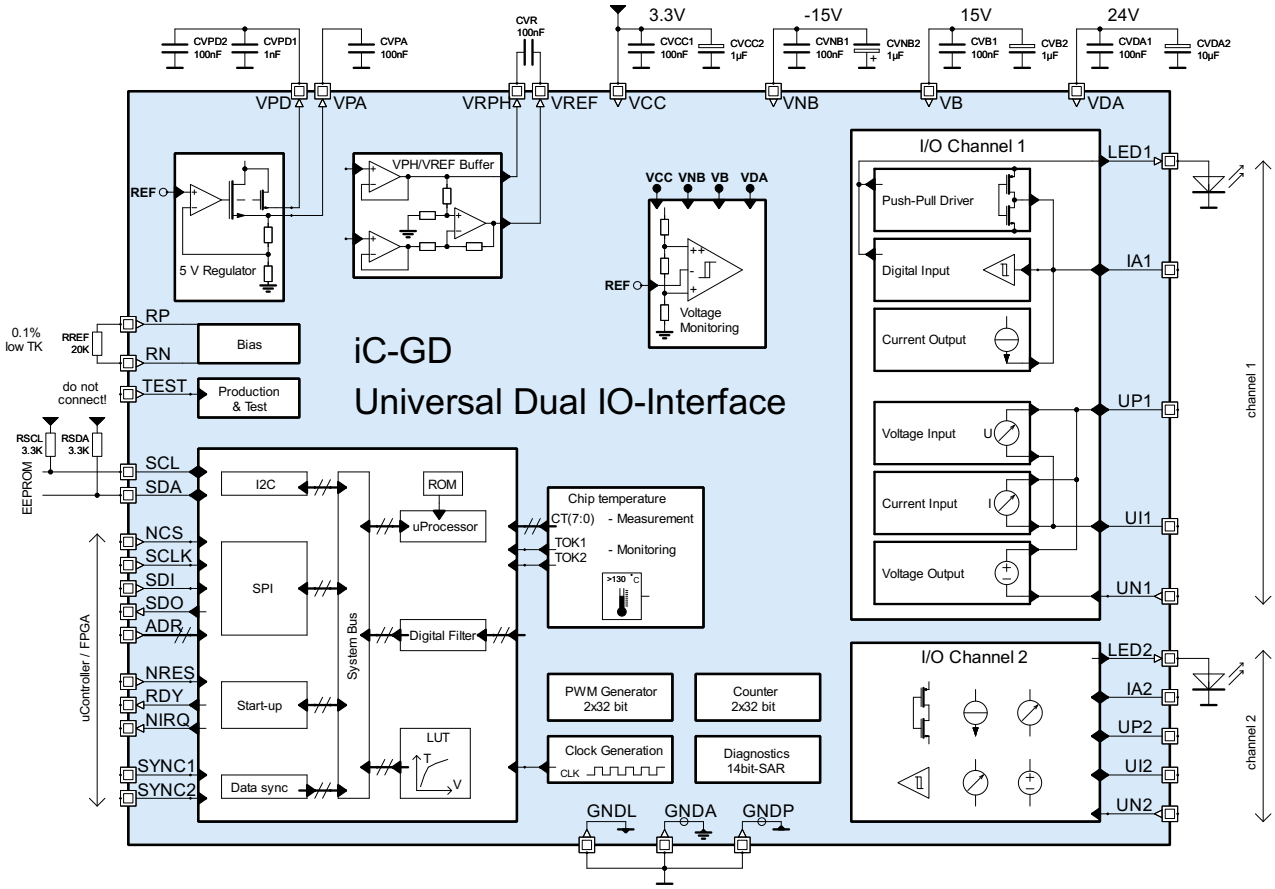


Figure 1: Typical external circuitry

CONNECTIVITY

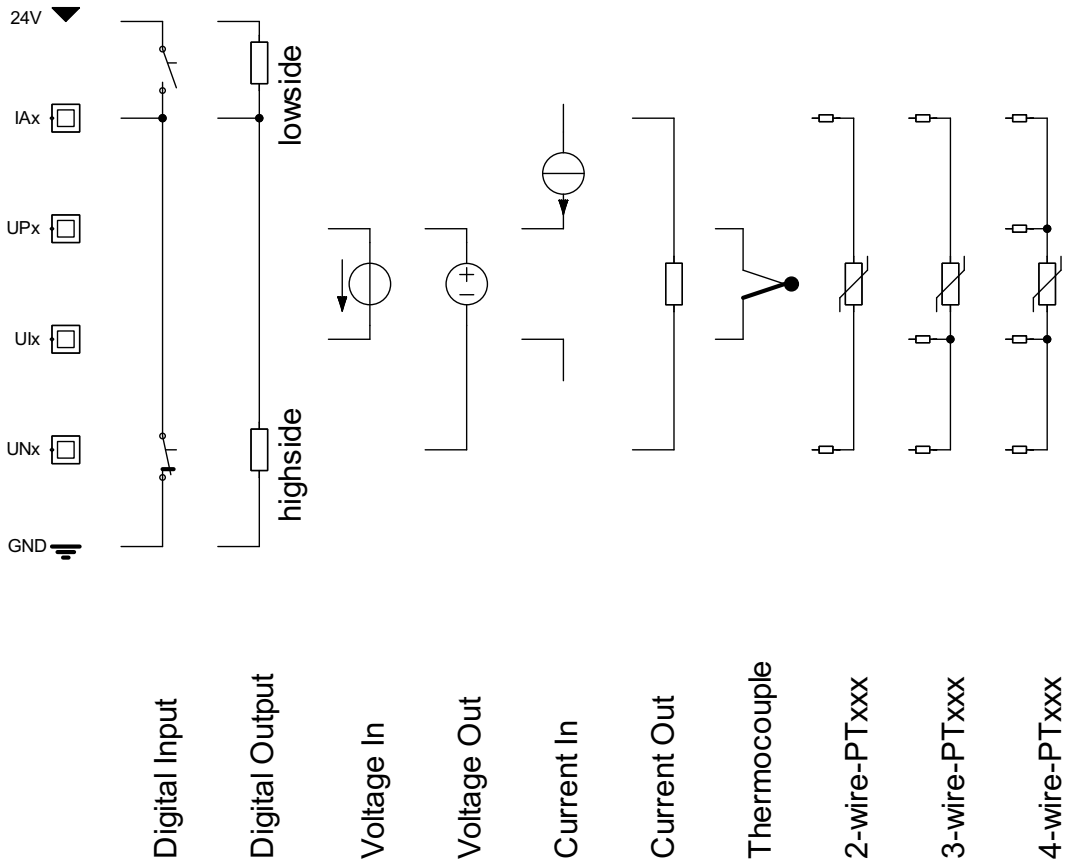


Figure 2: Overview of external connectivity

FUNCTION DESCRIPTION

Power supply
The iC is supplied via the following pins:

Power Supply			
Pin Name	Function	Range	typ. Value
VB	positive analog supply	14.5...16 V	+15 V
VNB	negative analog supply	-16...-14 V	-15 V
VCC	positive digital supply	3.135...5.25 V	3.3 or 5 V
VDA	positive power supply	18...36 V	24 V
GNDP	power ground	0 V	0 V
GNDL	logic ground	0 V	0 V
GNDA	analog ground	0 V	0 V

Table 4: Power Supply

The pins GNDP, GNDL and GNDA are to be connected externally via a neutral point.

Default state of IO pins
- IAx: Configured as digital type 3 inputs according to DIN/EN 61131-2
- UPx: Configured as voltage outputs with 0 V vs. UNx
- UIx: Pulldown current vs. VNB
- UNx: Pulldown current vs. GND

Digital inputs IAx
For the digital inputs several pull-down currents according to DIN/EN61131-2 and a pull-up current can be set. The status of the digital inputs can be indicated via LEDs to ground at the pins LEDx even if the iC is not supplied with voltage. In order to reduce power dissipation, the pull-down current flows through the LEDs to ground. If no LED is used, the corresponding LEDx pin must be connected to ground.

Digital outputs IAx
The digital outputs can be configured as low-side, high-side or push-pull drivers. If they are not configured as digital outputs they remain high-impedance.

The outputs are current-limited and switch off when the upper over-temperature limit T2 is reached. When the lower over-temperature limit T1 is exceeded, only the channel with excessive ouput current is disconnected.

A freewheeling circuit for inductive loads limits the positive voltage versus GNDP and the negative voltage versus VDA.

Diagnostics allow measuring and monitoring the output current in the output transistors directly. With appropriately configured pull-up or pulldown currents and voltage comparators, the status (output on or off, line break or short circuit to GNDP or VDA) can be detected.

Analog inputs (UPx, UIx)
Table 5 shows the possible measuring ranges. The maximum ratings marked by (*) only apply, if the channel is configured as plain voltage input (IO_SEL_x = VI). Then the entire range is valid. If the channel is configured as temperature sensor (IO_SEL_x = TM), the maximum ratings in table 10 apply. The inputs include cable-break detection. The current inputs are current limited to protect the measuring resistor. In addition, it is possible to implement floating voltage or current measurements (e.g. floating thermocouples).

The individual measuring range must be calibrated to reach the specified accuracy. The accuracy according to the characteristics S02 to S05 is summarized in table 6.

Measuring ranges			
Range	**Maximum ratings**	**Digital values**	**Valid Range**
±10 V	-10.5000 V 10.4997 V	0x8000 0x7FFF	0x8619 ... 0x79E7
±1 V	-1.05000 V 1.04997 V	0x8000 0x7FFF	0x8619 ... 0x79E7
±100 mV	-105.000 mV 104.997 mV	0x8000 0x7FFF	0x8619 ... 0x79E7
±10 mV	-10.5000 mV 10.4997 mV	0x8000 0x7FFF	0x8619 ... 0x79E7
-17.5 mV... 87.5 mV (thermo couples JKTNE)	-17.5 mV 87.498 mV	0x8000 0x7FFF	0x8000 ... 0x7FFF (*)
-4.375 mV... 21.875 mV (thermo couples RSB)	-4.375 mV 21.8747 mV	0x8000 0x7FFF	0x8000 ... 0x7FFF (*)
±20 mA	-21 mA 20.999 mA	0x8000 0x7FFF	0x8619 ... 0x79E7
4... 20 mA	-13 mA 4 mA 20.999 mA	0x8000 0x0000 0x7FFF	0x0000 ... 0x7878

Table 5: Measurement ranges of the analog inputs

Accuracy of measuring ranges			
Tj	**25 °C**	**-40...100 °C**	**-40...120 °C**
±10 V	5.25 mV	21 mV	42 mV
±1 V	0.525 mV	2.1 mV	4.2 mV
±100 mV	52.5 µV	210 µV	420 µV
±10 mV	5.25 µV	21 µV	42 µV
-17.5 mV... 87.5 mV	26.25 µV	105 µV	210 µV
-4.375 mV... 21.875 mV	6.56 µV	26.25 µV	52.5 µV

Table 6: Accuracy of the measurement ranges depending on chip temperature

Analog outputs (UPx, UNx, IAx)
The positive voltage outputs UPx are current-limited and switch off, when overtemperature limit T2 is exceeded. If the temperature exceeds overtemperature limit T1, the output is only disconnected, if it reports an overload at the same time.

An extended current mode provides increased current capability of up to +20 mA.

All negative voltage outputs UNx contain a 25 mA current source that only switches off in case of overload and when exceeding the upper overtemperature limit T2.

When the short-circuit output current is reached, a seperate error bit is set for each of the states *low* and *high*. An overload is reported when the output voltage deviates from the set point by more than 1 V, since a short circuit can occur anywhere in the entire output voltage range.

In combination with an external resistor and the voltage measurement (*Mixed Mode*), the current outputs IAx can be extended for a resistance measurement. The measuring ranges and tolerances are the same as for the individual functions. The minimum supply voltage VB = 14.5 V and the saturation voltage hi at the output IAx result in a maximum load of 600 Ω for 20 mA current output.

By reaching the upper dynamic range, a high-impedance load or open wire at IAx or UIx during a 3-wire measurement can be detected. This is indicated by the relevant error bits. For this functionality, at least one output current of -10 mA must be set. If an NTC or PTC resistance is used for temperature measurement, the linearization and calibration must be carried out externally.

Both voltage and current outputs must be calibrated to reach the specified accuracy. The accuracy according to the characteristics O02 to O05 is summarized in table 8.

Output ranges		
Range	**Maximum ratings**	**Digital values**
±10 V	-10.500 V 10.499 V	0x8000 0x7FFC
0...20 mA	0 mA 20.999 mA	0x0000 0xFFFC
4...20 mA	4 mA 20.999 mA	0x0000 0xFFFC
0...2 mA	0 mA 2.0999 mA	0x0000 0xFFFC
0...200 µA	0 mA 209.99 µA	0x0000 0xFFFC

Table 7: Output ranges of the analog outputs

Accuracy of output ranges			
Tj	**25 °C**	**-40...100 °C**	**-40...120 °C**
±10 V	5.25 mV	21 mV	42 mV
0...20 mA	42 µA	84 µA	168 µA
4...20 mA	34 µA	68 µA	136 µA
0...2 mA	4.2 µA	8.4 µA	16.8 µA
0...200 µA	0.42 µA	0.84 µA	1.68 µA

Table 8: Accuracy of the output ranges depending on chip temperature

Thermocouples and PT temperature sensors
Table 10 shows the supported thermocouples and PT temperature sensors. The temperature is determined with a resolution of 0.1 K.

To calculate the temperature of the thermocouples at the measuring point, the cold junction temperature is also required. The cold junction temperature needs to be stored as a digital value in the range of -20...105 °C for both channels and in the same format as the temperature itself via the SPI in the register TEMP_KSK.

The cold junction temperature is limited internally to its valid range. The linearization of the measuring temperature continues, even when leaving the valid temperature range (see table 10). This prevents an overflow of the number range. Additionally, the negative range is limited to -209.15 °C. The upper and lower values of temperature range apply as threshold values for the range excess. This is compared to the final calculated temperature, i.e. for the thermocouples after cold junction compensation. Table 65 shows by way of example further settings for additional PT features for which linearization can also be used. The accuracy according to the Electrical Characteristics Item No. S06 is summarized in table 11.

Temperature range		
Range	**Maximum ratings**	**Digital value**
Thermo couple, PT sensor	0 K 6,553.5 K	0x0000 0xFFFF

Table 9: Temperature range

Thermo couples		
Typ	**Temperature range**	**Valid range**
J	-100...1200 °C	0x06C4...0x398B
K	-100...1370 °C	0x06C4...0x402F
T	-100...400 °C	0x06C4...0x1A4B
N	-100...1300 °C	0x06C4...0x3D73
E	-100...1000 °C	0x06C4...0x31BB
R	-50...1768 °C	0x08B8...0x4FBB
S	-50...1768 °C	0x08B8...0x4FBB
B	600...1820 °C	0x221C...0x51C3
PT sensors		
Typ	**Temperature range**	**Valid range**
PT-100	-100...800 °C	0x06C4...0x29EB
PT-1000	-100...800 °C	0x06C4...0x29EB

Table 10: Temperature measurement

Accuracy of the temperature ranges			
Tj	**25 °C**	**-40...100 °C**	**-40...120 °C**
TE Type J	1.95 °C	3.9 °C	7.8 °C
TE Type K	2.21 °C	4.41 °C	8.82 °C
TE Type T	0.75 °C	1.5 °C	3.0 °C
TE Type N	2.1 °C	4.2 °C	8.4 °C
TE Type E	1.65 °C	3.3 °C	6.6 °C
TE Type R	2.73 °C	5.45 °C	10.9 °C
TE Type S	2.73 °C	5.45 °C	10.9 °C
TE Type B	1.83 °C	3.66 °C	7.32 °C
PT100, PT1000	1.35 °C	2.7 °C	5.4 °C

Table 11: Accuracy of the temperature ranges depending on chip temperature

Diagnostic measurements
For diagnostic purposes, several voltages and the currents in the outputs IAx as well as internal reference voltages can be measured by a 14 bit ADC. The converter maps the voltage range of 0 to 5.25 µA or 0 to 60 µA respectively with a 14-bit resolution to the digital values DAC[13:0] of 0x0000 to 0x3FFF. Due to internal limitations, the actual usable measuring range is lower as shown in table 12.

Diagnostic measurements		
Name	**Conversion**	**Measurement range**
+15 V supply voltage VB	$\frac{5.25\,V}{2^{14}} \cdot DIAG \cdot 6$	0...18 V
-15 V supply voltage VNB	$\frac{5.25\,V}{2^{14}} \cdot DIAG \cdot 6 - 26.25\,V$	-18...-8.25 V
3.3...5 V supply voltage VCC	$\frac{5.25\,V}{2^{14}} \cdot DIAG \cdot 2$	0...6 V
24 V supply voltage VDA	$\frac{5.25\,V}{2^{14}} \cdot DIAG \cdot 12$	0...36 V
5.25 V supply voltage analog VPA	$\frac{5.25\,V}{2^{14}} \cdot DIAG \cdot 2$	0...6 V
5.25 V supply voltage digital VPD	$\frac{5.25\,V}{2^{14}} \cdot DIAG \cdot 2$	0...6 V
Current from digital hi-side output IAx	$-\frac{60\,\mu A}{2^{14}} \cdot DIAG \cdot 10000$	-600...0 mA
Current into digital lo-side output IAx	$\frac{60\,\mu A}{2^{14}} \cdot DIAG \cdot 10000$	0...600 mA

Table 12: Diagnostic measurements

EEPROM

Batch number and one-time programming
During production, a 24-bit serial number is stored on the chip. It is composed of the batch, wafer and chip number and can be read via SPI. In addition, the temperature coefficient of the bandgap (ATK), the temperature coefficient of the chip's internal resistor for current measurement (AITKQ, AITKL) and the offset of the chip temperature measurement (AOCT) are calculated and stored (OTP).

EEPROM
The following table describes the structure of the data in the EEPROM starting at the top left with address 0x00. Every cell represents one byte.

Configuration								
00-07	(unused)	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)
08-0F	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)
10-17	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)
18-1F	(RES)	(RES)	(RES)	(RES)	(RES)	(RES)	CRCX	
Calibration								
20-27	ATK	AITKL	AITKQ_AOCT	AGVP1h	AGVN1h	AGVP2h	AGVN2h	AOGVsxl
28-2F	AOIA1	AOIA2	AOSZ	(unused)			CRCY	
30-37	AGIAA1	CRCA1	AGIAB1	CRCA1	AGIAC1	CRCA1	AGIAD1	CRCA1
38-3F	AGIAA2	CRCA2	AGIAB2	CRCA2	AGIAC2	CRCA2	AGIAD2	CRCA2
40-44	AGFA1		AOFA1		CRCFA1			
45-49	AGFB1		AOFB1		CRCFB1			
4A-4E	AGFC1		AOFC1		CRCFC1			
4F-53	AGFD1		AOFD1		CRCFD1			
54-58	AGFE1		AOFE1		CRCFE1			
59-5D	AGFF1		AOFF1		CRCFF1			
5E-62	AGFG1		AOFG1		CRCFG1			
63-67	AGFH1		AOFH1		CRCFH1			
68-6C	AGFA2		AOFA2		CRCFA2			
6D-71	AGFB2		AOFB2		CRCFB2			
72-76	AGFC2		AOFC2		CRCFC2			
77-7B	AGFD2		AOFD2		CRCFD2			
7C-80	AGFE2		AOFE2		CRCFE2			
81-85	AGFF2		AOFF2		CRCFF2			
86-8A	AGFG2		AOFG2		CRCFG2			
8B-8F	AGFH2		AOFH2		CRCFH2			
User space								
90-FF	at free disposal							

Table 13: Register assignment EEPROM

Configuration
The first EEPROM memory area contains the configuration. The configuration is written exclusively via SPI using register WR_EEPROM_CONF. In addition to the configuration data marked with (RES), the correct CRC value CRCX is also calculated and written.

Calibration
The calibration data for the absolute accuracy and the matching CRCs is written via SPI using opcode I^2C TRANSFER. It serves to calibrate production related tolerances and needs to be calculated only once.

The first data area up to CRCY contains the permanent calibration data that is read during start-up. The CRC value CRCY is calculated via the polynomial

$x^{16} + x^{14} + x^{12} + x^{11} + x^8 + x^5 + x^4 + x^2 + x^0$ (0x15935)

with the start value of 0xFFFF.

The second data area following CRCY contains configuration data that is required only in specific modes. It is read selectively when required. To ensure a secure transmission of data, these data is protected in small groups with 8 bit CRC values.

The polynomial used is

$x^8 + x^5 + x^3 + x^2 + x^1 + x^0$ (0x12F)

with a start value of 0xFF.

The four calibration values ATK, AITKO, AITKL and AOCT are calculated during chip production and stored internally (OTP). Via the configuration bit SEL_ETK, it is possible to choose between internal (OTP) and external (EEPROM) calibration during start-up. In both cases, the values that are stored in the EEPROM are included in the CRC calculation. If the EEPROM value is not used by ATK, it must be set to the default value.

Description of the data in the EEPROM
In the register AOGVsxl, the LSBs of each 9 bit register AGVP1, AGVN1, AGVP2, and AGVN2 are organized as follows:

AGVP1 = AGVP1h & Bit3 (AOGVsxl)
AGVN1 = AGVN1h & Bit2 (AOGVsxl)
AGVP2 = AGVP2h & Bit1 (AOGVsxl)
AGVN2 = AGVN2h & Bit0 (AOGVsxl)

In addition, the register AOGVsxl contains the register AOV as follows:

AOV = Bit6:4 (AOGVsxl)

The register AITKQ_AOCT is divided as follows:

AITKQ = Bit7:5 (AITKQ_AOCT)
AOCT = Bit4:0 (AITKQ_AOCT)

Description m	
A	Current output 0...20 mA
B	Current output 4...20 mA
C	Current output 0...2.0 mA (≙ PT100)
D	Current output 0...200 µA (≙ PT1000)

Table 14: Description m (Tab. 16)

Description n	
A	Voltage input ±10 V
B	Voltage input ±1 V
C	Voltage input ±100 mV
D	Voltage input ±10m V
E	Voltage input -17.5...87.5 mV
F	Voltage input -4.375...21.875 mV
G	Current input -20...20 mA
H	Current input 4...20 mA

Table 15: Description n (Tab. 16)

Name	Description	Default value	Digit	Interpretation/correction faktor
ATK	Bandgap temperature coefficient	0x40	unsigned	1 LSB ≈ -0.6...-0.2 mV (non-linear)
AITKL, AITKQ	Current measurement (linear, square) temperature coefficients	0x00	unsigned	$1 + \frac{AITKL * CHIP\_TEMP}{2^{18}} - \frac{AITKQ * CHIP\_TEMP^2}{2^{22}}$
AOCT	Chip temperature offset	0b00000	signed (2 K)	1 LSB = 1 K
AOSZ	Oscillator offset, left-aligned (i.e. 0xFE in EEPROM)	0x7F	Bit 6 = sign Bit 5:0 = value	$1 + \frac{AOSZ}{c_1}$, c_1 = 192 *for* $AOSZ \geq 0$ $\frac{1}{1 - \frac{AOSZ}{c_2}}$, c_2 = 180 *for* $AOSZ < 0$
AGVPx	Positive voltage output gain	0x100	unsigned	$\frac{\frac{R_G}{R_A} + 0.5}{\frac{R_G}{R_A} + \frac{AGVPx}{2^9}}$, $\frac{R_G}{R_A}$ = 19.2
AGVNx	Negative voltage output gain	0x100	unsigned	$\frac{\frac{R_G}{R_A} + 0.5}{\frac{R_G}{R_A} + \frac{AGVNx}{2^9}}$, $\frac{R_G}{R_A}$ = 19.2
AOIAx	Current output 4...20 mA offset	0x80	unsigned	$\frac{\frac{R_G}{R_A} + 0.5}{\frac{R_G}{R_A} + \frac{AOIAx}{2^8}}$, $\frac{R_G}{R_A}$ = 15.5
AOV	Voltage output offset (valid for CH_1 and CH_2)	0b000	unsigned	1 LSB = 1.28 mV
AGIAmx	Current output gain, for m see Tab. 14, minus offset at 4...20 mA	0x80	unsigned	$\frac{\frac{R_G}{R_A} + 0.5}{\frac{R_G}{R_A} + \frac{AGIAmx}{2^8}}$, $\frac{R_G}{R_A}$ = 16.6
AGFnx	Voltage/current input gain, for n see Tab. 15	0xDE7A	signed (2 K)	$X = \left(1.5 + \frac{AGFnx}{2^{15}}\right) * (X' + AOFnx)$
AOFnx	Voltage/current input offset, for n see Tab. 15	0x0000	signed (2 K)	(see AGFnx)

Table 16: Description of EEPROM data

CALIBRATION

Bandgap

The adjustable on-chip, second-order temperature-compensated bandgap is the voltage reference of the iC-GD. For adjusting the voltage reference, the parameter with the lowest temperature coefficient is calculated. This value is calculated during the production process and stored on-chip (OTP). It can be overwritten by a value stored in the external EEPROM. A bandgap voltage voltage that is too low is indicated in the supervisory register SPV_INT.

Bias

The reference current of the iC-GD is generated by an external resistor, RREF, between the pins RP and RN. To achieve a high accuracy of the current outputs, a resistor with a low temperature coefficient is required. The absolute value is not critical, but must not exceed ±1% to remain within the calibration range of the current outputs. The current in the resistor is monitored and the status is indicated in the supervisory register SPV_REG. When leaving the tolerance range, it switches to an on-chip generated current. To prevent voltage drop on the supply line and bond wire at pin RN, this pin must not be connected externally to ground.

Clock

An adjustable, internal oscillator generates a 2 MHz clock with a low temperature coefficient. A PLL multiplies this by the factor of 8 for use as the µC system clock. This PLL is also monitored and its status signalled in the supervisory register SPV_INT.

Calibration

The required calibration values can be transferred to the iC-GD in two different ways:

1. The calibration values are written via I^2C directly into the EEPROM. These changes are not directly transfered to the chip and require a restart (changing the mode will only be sufficed for calibration data that is reloaded selectively on demand i.e. AGIAmx, AGFnx, AOFnx).
2. The calibration values are written directly into the on-chip registers via SPI. Since these registers are not accessible in regular operation, the calibration mode must be activated. After all required calibration data have been calculated, they are also written into the EEPROM.

Calibration mode is activated by the register SPI_LOCK_RESET. If calibration mode is active, the internal register addresses used for the SPI communication differ partly from the valid addresses. If registers other than the calibration registers must be used, calibration mode must be deactivated again by the register SPI_LOCK_RESET. The remaining opcodes, including those for the transmission of process data, remain fully functional. Table 17 shows the valid internal addresses for calibration mode.

Name	Internal address	Hints and further settings
ATK	0x2C	
AITKL	0x69	
AITKQ, AOCT	0x7F	AITKQ: bits(7:5), AOCT: bits(4:0)
AOSZ	0x68	Requires a waiting time of 200 µs after writing
AGVP1h	0x28	
AGVN1h	0x29	
AGVP2h	0x2A	
AGVN2h	0x2B	
AGVsxl	0x1F	
AOIA1	0x1E	
AOIA2	0x2F	
AGIAm1	0x1D	
AGIAm2	0x2E	
AGFn1	0x0E – 0x0F	REG(0x0C) = 0x5C, REG(0x3A) = 0xFF (*)
AGFn2	0x0E – 0x0F	REG(0x0C) = 0x5D, REG(0x3A) = 0xFF (*)
AOFn1	0x0E – 0x0F	REG(0x0C) = 0x5E, REG(0x3A) = 0xFF (*)
AOFn2	0x0E – 0x0F	REG(0x0C) = 0x5F, REG(0x3A) = 0xFF (*)

Table 17: Internal calibration register addresses

(*) The order is relevant. First, the date, then the further settings in order as shown in table 15 must be set. Register 0x3A acts as trigger.

ATK – Bandgap TK
AOCT – Chip temperature measurement offset
AITKQ, AITKL – Current measurement resistor TK
The calibration of the bandgap, the chip temperature and the current- measurement resistor is performed during chip-production. The values are stored on-chip (OTP). A read access is possible via the register table according to table 17.

AOSZ oscillator
The calibration of the oscillator is done via the register AOSZ(6:0) in the range of approx. ±31.5% with a resolution of approx. 0.5%. To this end, a divided integer frequency of the internal clock (PWM) can either be output at the digital output IA1 or at pin SYNC1.

For output at IA1, the counter can be used in PWM mode. The output at the SYNC1 pin requires an additional command according to table 18. It shows the output of a 10 kHz signal at pin SYNC1 by way of example. Determined by the system, the first period is approx. 80 ns shorter when output at pin SYNC1.

The oscillator must not be operated over its nominal frequency, since this can crash the internal µC and cause data errors. Thus during start-up, the lowest possible frequency is used. When reading the frequency from the EEPROM after start-up, the value is only accepted if the respective CRC is correct.

There are no limitations for the calibration mode. For calibration, two iterations of the following equation with a start value of $AOSZ_0$ = -63 are usually required. Based on $AOSZ_n$ and f_{mess}, the respective valid equation must be selected (4 cases).

Attention should be paid to the format of AOSZ according to table 16 which does not represent a two's complement value. The start value corresponds to 0xFE (left-aligned, LSB unused, MSB = sign, remainder = value) in the EEPROM.

Command	Effect
BX 00 06	IO_SEL_1P = CNT
BX 01 43	SYNC_SEL_1 = DISO
BX 03 31	Counter value 1 = PWM in HS mode
DX 28 03200190	T_{ges} = 100 µs, T_{high} = 50 µs
0X 80	PROCESS DATA 1 = '1' (PWM on)
For additional output via SYNC1 only:	
BX 39 AA	Activate calibration mode
BX 25 80	Start output PWM → SYNC1
	* Measurement *
BX 25 00	Stop output PWM → SYNC1
BX 39 A5	Deactivate calibration mode

Table 18: Calibration AOSZ

Case 1: $AOSZ_n \geq 0, \quad AOSZ_n \geq c_1 * \left(\frac{f_{meas}}{f_{set}} - 1\right)$

$$AOSZ_{n+1} = AOSZ_n * \frac{f_{set}}{f_{meas}} + c_1 * \left(\frac{f_{set}}{f_{meas}} - 1\right)$$

Case 2: $AOSZ_n \geq 0, \quad AOSZ_n < c_1 * \left(\frac{f_{meas}}{f_{set}} - 1\right)$

$$AOSZ_{n+1} = \left(1 - \frac{f_{meas}}{f_{set}} * \frac{1}{1 + \frac{AOSZ_n}{c_1}}\right) * c_2$$

Case 3: $AOSZ_n < 0, \quad AOSZ_n \geq c_2 * \left(1 - \frac{f_{set}}{f_{meas}}\right)$

$$AOSZ_{n+1} = \left(\frac{f_{set}}{f_{meas}} * \frac{1}{1 - \frac{AOSZ_n}{c_2}} - 1\right) * c_1$$

Case 4: $AOSZ_n < 0, \quad AOSZ_n < c_2 * \left(1 - \frac{f_{set}}{f_{meas}}\right)$

$$AOSZ_{n+1} = AOSZ_n * \frac{f_{meas}}{f_{set}} + c_2 * \left(1 - \frac{f_{meas}}{f_{set}}\right)$$

with

$$c_1 = 192, \quad c_2 = 180$$

AOV – Voltage output offset
The output voltage offset calibration, UPx − UNx, is done for both channels via the 3-bit register AOV. The calibration range covers approx. 9 mV in steps of 1.28 mV.

With AOV = 0b000 at channel 1, a voltage of 0 mV (0x0000) is output and the (negative) offset is determined. The calibration value AOV then results in:

$$AOV = -\frac{V_{meas}}{1.28\,mV}$$

AGVsx – Voltage output gain
The output voltage gain calibration, UPx − UNx, is centrally carried out via the internal 5.25 V voltage reference of the 14-bit D/A converter. The calibration range based on the output voltage of ±10.5 V is approx. 512 mV in steps of approx. 1 mV.

For this, a previous calibration of the offset (AOV) is required.

The four calibration values AGVPx(8:0) and AGVNx(8:0) must be calculated for both channels and separately for the positive and negative output range. For start value $AGVsx_0$ = 0x100 and the maximum magnitude of voltage V_{set} must be performed:

$$AGVsx_{n+1} = AGVsx_n * \frac{V_{meas}}{V_{set}} + 2^9 * 19.2 * \left(\frac{V_{meas}}{V_{set}} - 1\right)$$

AOIAx – Current output offset
The current output offset applies to the 4 to 20 mA range only. The calibration range is approx. 0.25 mA. The calibration steps are approx. 1 µA.

The calibration is performed with IAx at 4 mA (0x0000) via AOIAx(7:0). For this, two iterations according to the following equation with the start value $AOIAx_0$ = 0x80 are performed:

$$AOIAx_{n+1} = AOIAx_n * \frac{I_{meas}}{I_{set}} + 2^8 * 15.5 * \left(\frac{I_{meas}}{I_{set}} - 1\right)$$

AGIAmx – Current output gain
The calibration range for the current output gain is approx. 6.1% (minus offset of the 4 to 20 mA range). The calibration steps are 1/256 (i.e. e.g. selected in the 0 to 20 mA range with 21 mA: calibration range approx. 1.28 mA, calibration steps approx. 5 µA).

For the calibration of the current output gain, a previous calibration of the current output offset (AOIAx, only in the range of 4 to 20 mA) is required.

The output current calibration at IAx is carried out for both output ranges of 0 to 20 mA as gain of the fullscale value of approx. 21 mA (0xFFC) via AGIAAx(7:0) or AGIABx(7:0).

For the ranges 0 to 2 mA or 0 to 200 µA, that are primarily intended for the PT100 or PT1000 measurement, the gain is calculated at 1.7 mA or 170 µA (both 0xCF3C) via AGIACx(7:0) or AGIADx(7:0). This value is used for energizing the PT elements and is stored on the chip. The calibration is made with in each case 2 iterations according to the following equation with the start value $AGIAmx_0$ = 0x80:

$$AGIAmx_{n+1} = AGIAmx_n * \frac{I_{meas} - I_{offset}}{I_{set} - I_{offset}}$$

$$+2^8 * 16.6 * \left(\frac{I_{meas} - I_{offset}}{I_{set} - I_{offset}} - 1\right)$$

AGFnx, AOFnx
The current/voltage measurement calibration is made for the different measuring ranges by setting the offset (AOFnx) and the gain (AGFnx). Required is a previous successful calibration of the voltage outputs.

At AGFnx = 0xC000 and AOFnx = 0x000, several voltage/current values are externally applied (X_{set}) and

read back via the SPI (X_{meas}). The two maximum values are used for all measuring ranges (value 1 and 2). In addition, for the symmetric measuring ranges, the offset at 0 V/0 mA (value 0) is determined. For the current measurement offset, also the current chip temperature and the temperature coefficient values AITKQ, AITKL are required. The latter are stored on the chip, see table 17. The required values are used unitless in the format of the process data: X_{set} und X_{meas} as signed numbers, and additionally for the current measurement AITKQ, AITKL and CHIP_TEMP, all as unsigned numbers.

The following four conditions must be kept:

$$\left(1.5 + \frac{AGFnx}{2^{15}}\right) * \left(AOFnx + 2^{15}\right) > 2^{15} - 1$$

$$\left(1.5 + \frac{AGFnx}{2^{15}}\right) * \left(AOFnx - 2^{15}\right) < -2^{15}$$

$$\left(1.5 + \frac{AGFnx}{2^{15}}\right) * AOFnx < 2^{15} - 1$$

$$\left(1.5 + \frac{AGFnx}{2^{15}}\right) * AOFnx > -2^{15}$$

3-point calibration (symmetrical ranges)
The following formulae are valid for the ranges ±10 V, ±1 V, ±100 mV, ±10 mV, ±20 mA.

Point 0 is calibrated exactly (to use for offset), point 1 and point 2 are calibrated best possible. The points should be distributed equidistantly.

Example
Point 0: 0 V, point 1: +10 V, point 2: -10 V.

$$AGFnx = \left(\frac{X_{set\,1} - X_{set\,0}}{X_{meas\,1} - X_{meas\,0}} + \frac{X_{set\,2} - X_{set\,0}}{X_{meas\,2} - X_{meas\,0}} - 3\right) * 2^{14}$$

$$AOFnx_{(VI)} = \frac{X_{set\,0}}{1.5 + \frac{AGFnx}{2^{15}}} - X_{meas\,0}$$

$$AOFnx_{(CI)} = \left(\frac{X_{set\,0}}{1.5 + \frac{AGFnx}{2^{15}}} - X_{meas\,0}\right) * \frac{1}{f_T}$$

2-point calibration (asymmetrical ranges)
The following formulae are valid for the ranges -17.5 mV to 87.5 mV, -4.375 mV to 21.875 mV, 4 to 20 mA. Point 1 and point 2 are to be adjusted exactly.

Example
Point 1: 4 mA, point 2: 20 mA.

$$AGFnx = \left(\frac{X_{set\,2} - X_{set\,1}}{X_{meas\,2} - X_{meas\,1}} - 1.5\right) * 2^{15}$$

$$AOFnx_{(VI)} = \frac{X_{set\,1} * X_{meas\,2} - X_{set\,2} * X_{meas\,1}}{X_{set\,2} - X_{set\,1}}$$

$$AOFnx_{(CI)} = \frac{X_{set\,1} * X_{meas\,2} - X_{set\,2} * X_{meas\,1} + c_0 * (f_T - 1) * (X_{set\,2} - X_{set\,1} + X_{meas\,1} - X_{meas\,2})}{(X_{set\,2} - X_{set\,1}) * f_T}$$

$$with \quad c_0 = 7710, \quad f_T = 1 + \frac{AITKL * CHIP\_TEMP}{2^{18}} - \frac{AITKQ * CHIP\_TEMP^2}{2^{22}}$$

STARTUP, RESET, WATCHDOGS

When the supply voltages are applied and VCC exceeds the undervoltage reset threshold (Vtu(VCC)hi), the iC-GD starts with the self-configuration. The internal registers are initialized and the configuration and calibration data from the EEPROM are read. During the phase of self-configuration, (RDY = lo), SPI communication is blocked.

The EEPROM is read via the I^2C interface. Here, the configuration and calibration data are read from the EEPROM and written into the internal registers. During the entire configuration, a 16-bit CRC checksum is calculated and compared with the checksum that is also stored in the EEPROM. If these do not match, the configuration will be rejected and the chip returns to its default state. The error status is stored in register SPV_REG, bit ST_CONF. Also, a 16-bit checksum is calculated for the calibration data and compared with the checksum stored in the EEPROM. If those do not match, only the error status is stored in the register SPV_REG, bit ST_CALIB. The read data is kept, except for the frequency calibration. Additionally, in certain modes further calibration data from the EEPROM is read and protected by a separate 8-bit CRC if required.

The iC uses the memory area of the EEPROM shown in table 13. The subsequent memory area is freely available to the user.

The chip then provides several possibilities for internal and external resetting. The cause of the last reset is stored in a status register.

- **Supply voltage:** If the supply voltage VCC drops below the undervoltage reset threshold (Vtu(VCC)lo), the chip is reset. As stated above, it restarts when the supply voltage is restored.
- **NRES pin:** If the NRES pin is low for at least tRESlo, the chip is reset. Shorter pulses may but do not have to cause a reset.
- **Reset via SPI:** The chip can be reset immediately by writing into the register SPI_LOCK_RESET the relevant command.
- **Watchdog SPI:** An internal watchdog timer can be optionally enabled, to monitor the SPI communication. If no valid SPI communication takes place during a certain time period (see table 19), the watchdog resets the iC. A valid communication is one of the opcodes "PROCESS DATA 1/2/1 and 2".
- **Watchdog µC**: An internal watchdog monitors the internal processor. The processor operates the watchdog regularly during its main routine. If the watchdog is not operated within the the µC time-out (see table 19), it resets the iC.

Reset times	
Watchdog µC	125 ms ±5 ms
Watchdog SPI	53 ms ±3 ms

Table 19: Watchdogs (times are only valid with calibrated oscillator)

SPI

The iC-GD is controlled via an SPI interface. The SPI interface allows fast reading of measurement data and the setting of actuator values as well as reading and writing of configuration registers. The SPI provides a bridge to the I^2C interface and thus also to the connected EEPROM.

The SPI operates synchronously with the supplied clock. To this end, it samples the input data with the falling edge and outputs the data with the rising edge. By default, it outputs the input data with half a clock delay. The iC is activated by the NCS pin, so that the subsequent 8 bits can be interpreted as control code. This contains a 4-bit opcode, a 3-bit address and a broadcast bit. If the iC as such is not addressed, it *hibernates* and only relays the input data. Otherwise, it interprets the opcode.

An additional delay in the signal path (SDO) between 0 and 7 clocks can be set via the configuration bit EN_UCM. Thus, the total delay of a daisy chain of up to 8 iCs can be set up to a multiple of 8 clocks. This has to be carried out in the last iC of the SPI chain. This iC automatically determines the required number of clocks of additional delay by means of its address. This allows proper control by a µC.

The SPI protocol is optimized for the transfer of sensor and actuator data. Sensor data is available directly following the opcode and can be clocked out subsequently. Actuator data can be sent directly following the opcode. To read data from internal registers, a provisioning time of 8 clocks following the opcode and the address is required, which can be filled with optional data. To write register data, no *padding* is required by the SPI. When

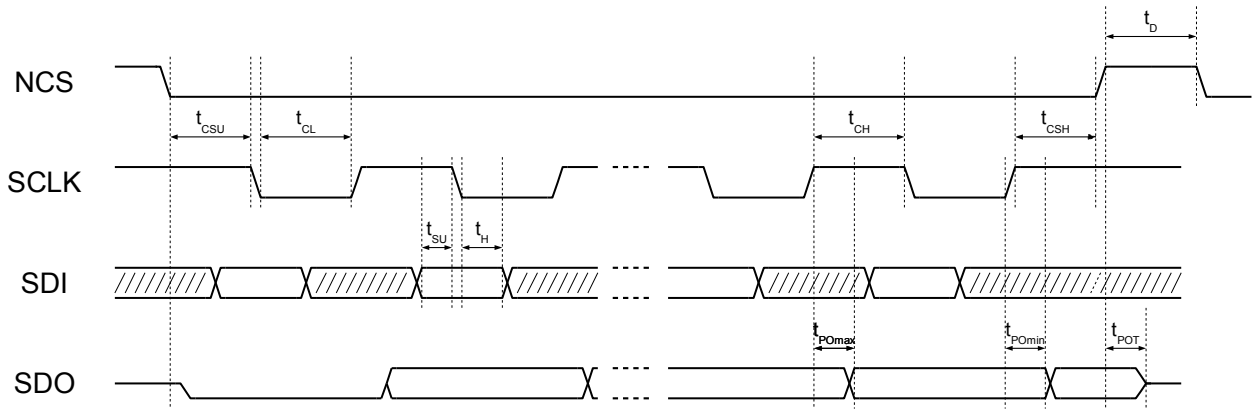
reading and writing data via I^2C, e.g. to the EEPROM, one has to poll for the end of this process before a new I^2C communication can be started.

In addition, the SPI provides opcodes as respective SYNC signals (edges and channels) and opcodes for fast reading of the registers CH_STAT_REG and IRQ_FLAG_REG. Figure 5 shows the SPI communication.

The SPI is blocked during the startup (RDY = 0). No communication is possible during this time. In normal operation, 30 µs after the beginning of startup at the latest (usually with the rising edge of NRES), NCS must be high. Otherwise the iC performs a quickstart that skips reading the EEPROM and the internal calibration data. In this case, both CRC error bits are set (see chapter *Calibration*).

Figure 3 shows the SPI timing. The given times are listed under operating conditions.

Figure 4 shows by way of example a daisy chain of three iCs with five active channels that are controlled by a µC. The input data noted above the iCs are sampled with the falling edge at NCS for all iCs simultaneously and then clocked out via SPI. The output data written by the SPI is noted below the iCs and is also output simultaneously with the rising edge at NCS for all iCs (for analog outputs: subsequently with the next refresh-cycle).



Daisy chain example

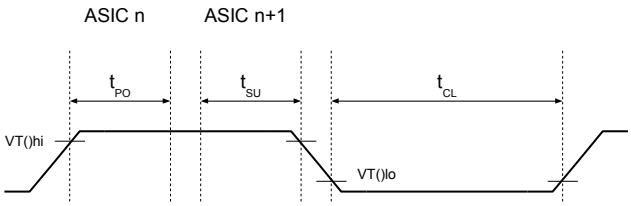


Figure 3: SPI-Timing

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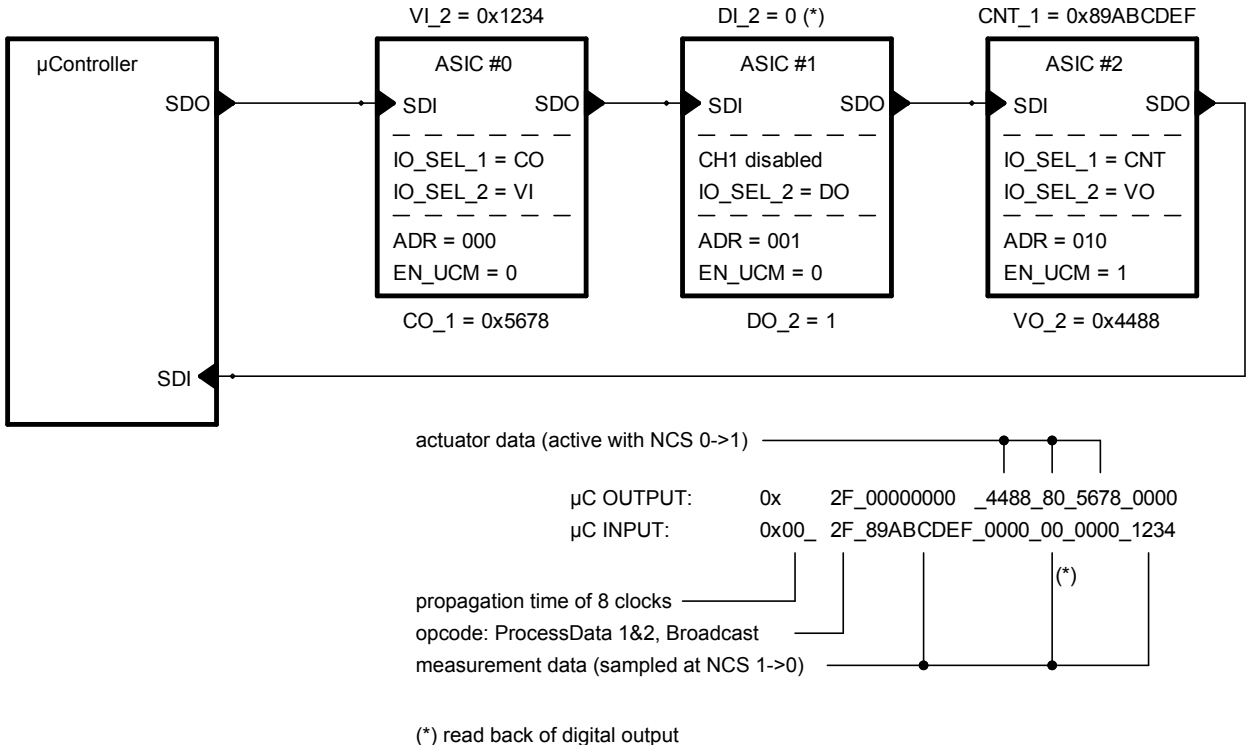

Figure 4: Example of a three iC daisy chain with five active channels

Figure 5: SPI Communication

COUNTER

Via the two digital inputs with their following spike filters, two 32-bit wide counters can be operated. In *single mode*, the counters are operated independently. In *dual mode* (see below), one counter is controlled by both inputs. The counters can also be used as PWM generators.

For each counter, one reference value can be configured that sets a status bit and causes an interrupt, when reached. In addition, a bit can be configured that determines whether an interrupt is caused once or every time the reference value is reached. In the latter case it can be reset via the register SPI_LOCK_RESET. This prevents the setting of a status bit and the triggering of an interrupt in case the counter fluctuates around the reference value or is at the reference value. The same functions are available for the second reference value and the overflow and underflow of the counter.

The bit CNT_RAR allows the configuration of a counter to be reset when the reference value is reached (*reset at reference*). The reference value itself is not reached though. Additionally, the input signal can be inverted prior to internal processing and the counting direction (up/down) be set in most counter modes.

The counters operate synchronously with the SYNC signal or asynchronously so that the current value is supplied. Some modes do not allow external synchronization because the respective synchronization is carried out internally. This affects the time measurement and the synchronization triggered by the second channel. The synchronous mode also allows reading the asynchronous (current) counter value by sending a SYNC command to the relevant iC via the SPI and reading the value as regular sensor data. Tab. 21 gives an overview of usable configuration bits depending on the selected mode. 'X' means 'possible', '-' means 'not possible' (bit is ignored), '(-)' means 'possible but not useful'.

Additionally, the counter allows the generation of a pulse-width modulated signal in two different modes.

- **Simple PWM**: The PWM mode is selected and both 16 bit periods t_high and t_ges as in Table 20 and Figure 6 are written to the reference register. The PWM can be switched on and off via the process data. When switched on, it re-starts its period with '1'. In addition, the pulse-width can be changed during run-time by writing the lower half of the reference register. In this case, a period that has already started internally is completed and then the new value is adopted. When the cycle time is changed, the current period is terminated immediately and a new period is started.
- **PWM with activation pulse**: Unlike in simple PWM mode, an *activation pulse* is generated at startup before the PWM automatically switches to the regular PWM mode. Note: The registers are interpreted differently than the simple PWM mode (see Figure 6). A change of the pulse width is not intended in this mode. It is possible though by writing the entire SET_CNT register with 0x0000 in the upper half. In contrast to the simple PWM mode, here the period will not be completed but starts immediately with a new period. When the cycle time is changed, the current period is terminated immediately and a new period is started without a new activation pulse.

In both modes, the PWM mode supports a high-speed mode (HS) with a resolution of 125 ns, a cycle time of up to 8.192 ms and a low-speed mode (LS) with a resolution of 16 ns and a cycle time of up to 1.048 s (see Table 20). The initial pulse may be up to 1 LSB shorter due to the temporal resolution of the internal clock in low-speed mode. The reference register can either be written completely (4 bytes) or only its low-order part (2 bytes). For simple PWM, the latter complies with a change of t_high. The PWM then is output at IAx (X = 1, 2). Time t_ges must not be 0x0000.

These following modes are supported by the counters:

Single mode

- **Pulse counter:** Counts pulses (= rising edges) of the respective channel.
- **Time measurement period:** Measures the time between two rising edges. No external sync possible because it is synchronized with the rising edge.
- **Time measurement pulse width:** Measures the time that the respective channel is high. No external sync possible because it is synchronized with the falling edge.
- **Pulse-width modulation:** Generates a PWM signal with a duty cycle depending on REF_CNT_x. The High-time, cycle time and, if necessary, the activation pulse time are configurable (see figure 6).

Dual Mode

- **Pulse counter with trigger:** Counts pulses on CH_1. CH_2 serves as a trigger to enable the counter value to be output. The counter value CH_1 is not reset. Since CH_2 performs the function of synchronization, no external sync is possible.

- **Pulse counter with reset:** Counts pulses at CH_1. CH_2 acts as reset input. While CH_2 is high, the counter is reset.
- **Pulse counter with gated signal:** Counts pulses at CH_1, if CH_2 is high.
- **Pulse counter with direction signal:** Counts pulses at CH_1, positive for CH_2 = 0, negative for CH_2 = 1.
- **Time measurement edge to edge between channel 1 and 2:** Measures the time of the rising edge at CH_1 to the rising edge at CH_2. In case of several consecutive rising edges at CH_1, the last one (minimum time) is measured. In case of several consecutive rising edges at CH_2, the time to the last rising edge of CH_1 is measured. If both edges rise simultaneously (within the sampling resolution), the time to the preceding rising edge of CH_1 is measured, (i.e. not 0). CH_2 acts as synchronization input, no external sync possible.

- **Incremental encoder** with single, dual and quadruple evaluation.

Mode	Resolution LSB	Maximum time
Time measurements	125 ns	537 s
PWM, HS mode	125 ns	8.192 ms
PWM, LS mode	16 µs	1.048 s

Table 20: Counter times

Mode	SYNC	CBE	DNU	RAR	DCB
Pulse counter	X	X	X	X	X
Time measurement period	-	-	-	(-)	X
Time measurement pulse width	-	-	-	(-)	X
Pulse counter with trigger	-	X	X	X	X
Pulse counter with reset	X	X	X	X	X
Pulse counter with Gate	X	X	X	X	X
Pulse counter with direction signal	X	X	-	X	X
Time measurement CH1 → CH2	-	-	-	(-)	X
Incremental encoder 1 x	X	-	-	(-)	X
Incremental encoder 2 x	X	-	-	(-)	X
Incremental encoder 4 x	X	-	-	(-)	X

Table 21: Overview of the usable counter setting bits

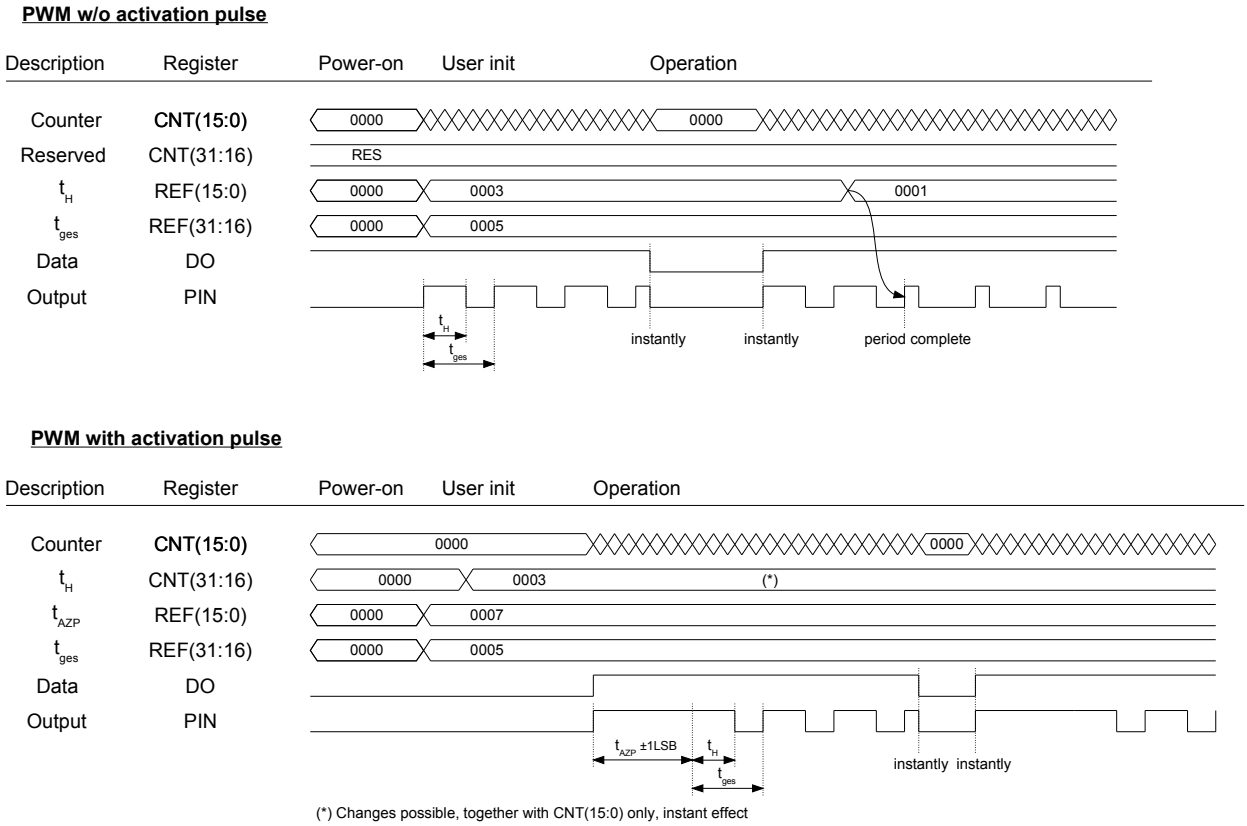

Figure 6: Register interpretation and PWM modes

MIXED OPERATION

Provided that functions do not overlap, two operating modes can be used on one channel simultaneously. The pins IA1 and IA2 are available as digital input or output pins or current outputs if only the analog voltage inputs, the voltage outputs or the current input function at the particular channel is used. 4-wire PT temperature sensors require a current output IAx and a differential voltage input. A voltage output in conjunction with a 2- or 3-wire PT temperature sensor on one channel is not possible. The counter (only available as the primary function) complies with the digital input, the PWM complies with a digital output.

The primary function enables a fast data transfer via SPI command. The secondary function is only able to transfer data via register access and therefore is slower.

The following table shows all possible operating modes.

Possible mixed operating modes (primary and secondary function)										
Function **secondary** / **primary**	Digital input	Digital output (*)	Voltage input	Current input	Voltage output	Current output	Counter	PWM (*)	Thermo couples	2, 3, 4-wire PTxxxx
Digital input			x	x	x					
Digital output *			x	x	x					
Voltage input	x	x				x		x		
Current input	x	x				x		x		
Voltage output	x	x				x		x		
Current output			x	x	x					
Counter			x	x	x					
PWM (*)			x	x	x					
Thermo couples	x	x				x				
2, 3, 4-wire PTxxxx						(x) (**)				

(*) The digital output can be digitally read back when operating as primary or secondary function. This is no mixed mode.

(**) When measuring PT, the iC automatically selects the current output as secondary function to provide the measuring current. Further use is not possible.

Table 22: Mixed operating modes

MONITORING

Voltage monitoring
The supply voltages VDA, VB, VNB, and VCC and the internally generated voltages VPA and VPD are monitored. If they fall below their respective thresholds, the corresponding error bits are set. If the digital out- and input is not used, VDA can also be supplied with VDA = VB = 15 V to omit the 24 V supply. Here, the bit VDA_VB must be set to avoid an alert of the VDA monitor. Alternatively, the relevant interrupt generation can be masked.

Chip-temperature measurement
The iC features a configurable internal 8-bit temperature-to-digital converter to measure the chip temperature. The temperature is available via SPI. The exact chip temperature is also required for the current measurement via a configuralbe internal resistor to account for its TK. Both calibrations are carried out during the chip production process and are stored internally (OTP). They can be overwritten with a value from the external EEPROM.

Overtemperature behavior
The iC features two-stage temperature monitoring. When the shutdown temperature T1 is reached, the digital outputs, the current outputs, and the voltage outputs are switched off if the relevant output cannot saturate and therefore is responsible for the overtemperature. When the shutdown temperature T2 is reached, all outputs are switched off. The outputs automatically restart, when the chip temperature falls below the restart temperature. The overtemperature detection T2 can be deactivated for test purposes.

Register setting
The iC features three registers for general supervision: The *supervisory register* (SPV_REG) indicates errors at the voltage supplies, excessive chip temperature and CRC errors at configuration or calibration. The two *channel-status registers* (CH_STAT_REG) contain information on the functions in use on each channel and the primary and secondary function. The *interrupt register* (IRQ_FLAG_REG) is combinatorial and indicates received interrupts. *Enable registers* allow masking of individual status bits.

Once set, error bits stay set, even if the error does not persist. The bits are reset during the reading of the particular register (RD + RST). If the error persists, the error bit is set again. If the transmission of individual bits is deactivated by entries of the particular *enable register*, the register is not touched. When the bits are activated, also previosly occured errors are transmitted. An overview is shown in Figure 7.

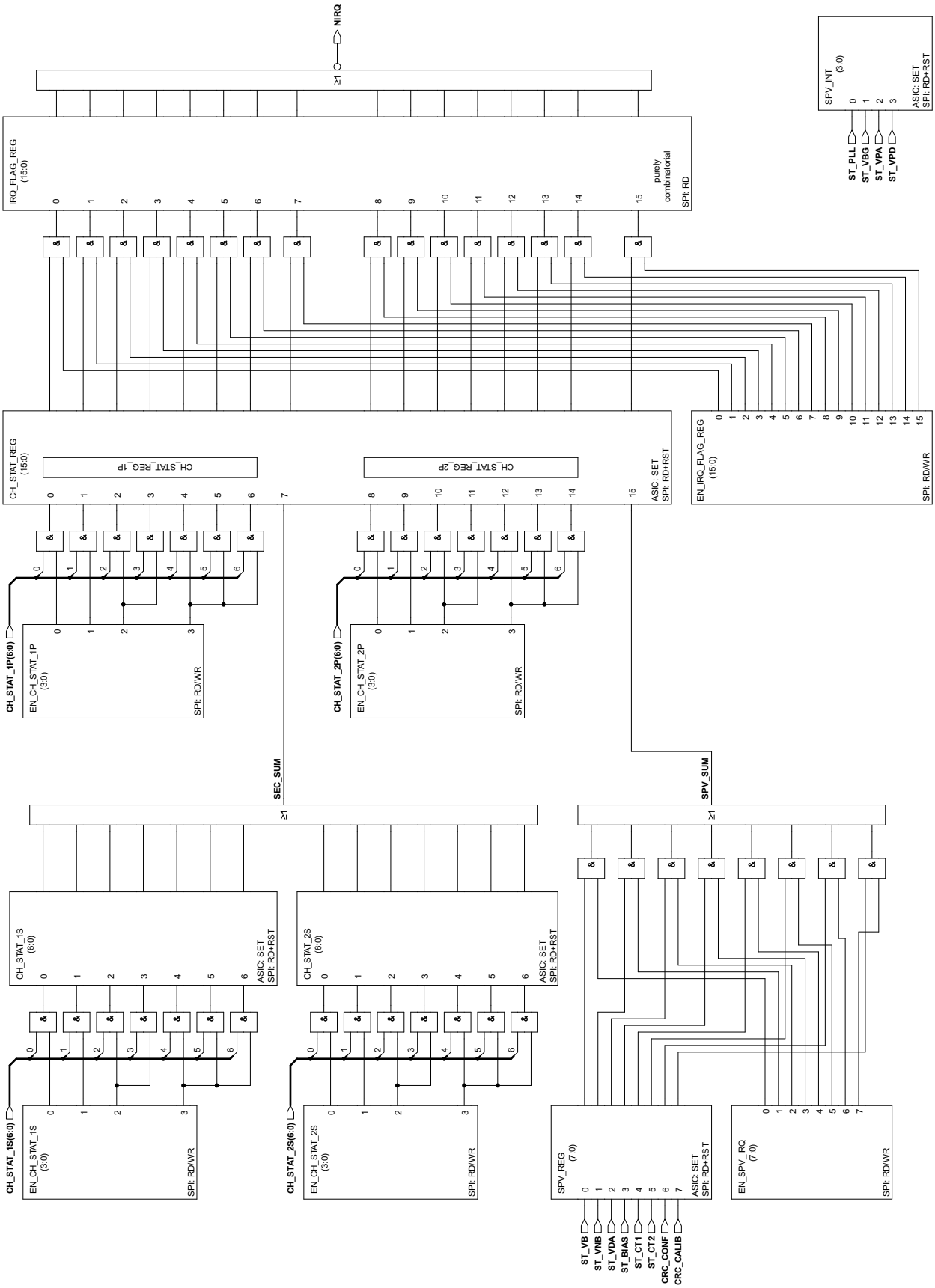

Figure 7: Overview *supervisory*, *channel status*, and *interrupt*

OPCODES

The first byte sent via SPI contains the address of the iC and the command. The address is defined by three bits that address the iC when they match its hard-wired address. A broadcast is also possible; here all chips are addressed and the address is ignored; the command defines the type of access. Possible are:

- **PROCESS DATA x:** The data of the primary channel is transmitted. The iC accepts the data when the addressed channel is configured as input. The iC outputs data when the addressed channel is configured as output. The bit width is adjusted automatically for the chosen mode.
- **READ CH_STAT_REG:** The *channel status register* is read, output and reset (RD + RST).
- **READ IRQ_FLAG_REG:** The *interrupt-flag register* is read and output. This way, the cause for an interrupt can be determined. It can be reset when no interrupt is indicated any more (formed combinatorial).
- **SYNC:** The current value is sampled and stored for channels that are configured as input (analog input, digital input, counter, temperature measurement). For channels that are configured as output, the last written value is output. The used edge can be configured per channel via the bit SYNC_INV_x. The Opcode *SYNC 1&2 – rising/falling edge* can reproduce a rising or falling edge and triggers synchronization only when the edge matches the configuration via SYNC_INV_x. The SYNC command has no effect if the channel does not operate synchronously (selectable via SYNC_SEL_x).
- **READ INTERNAL REGISTER (single):** The addressed register is output.
- **WRITE INTERNAL REGISTER (single):** The addressed register is written by the following byte.
- **READ INTERNAL REGISTER (continuous):** Operates like *single*; here the address is incremented automatically after each byte. This enables reading various consecutive registers. Usage in *broadcast* is not possible.
- **WRITE INTERNAL REGISTER (continuous):** Operates like *single*; here the address is incremented automatically after each byte. This enables the writing of consecutive register. Usage in *broadcast* is possible. All iCs accept the same data.
- **I²C TRANSFER/STATUS:** The *I²C TRANSFER* command allows addressing components connected to the iC via I²C. The iC operates as bridge. Therefore the regular commands of I²C are mapped. Details can be found in chapter *I²C*. Communication runs in the background. Via I²C STATUS can be polled for its completion.

Opcodes		
Bits	**Description**	**Values**
2:0	Address	0...7: Up to 8 chips individually addressable
3	Broadcast	0 = single 1 = broadcast (address irrelevant)
7:4	Command	0000 = PROCESS DATA 1P 0001 = PROCESS DATA 2P 0010 = PROCESS DATA 1P & 2P 0011 = READ CH_STAT_REG 0100 = READ IRQ_FLAG_REG 0101 = SYNC 1 0110 = SYNC 2 0111 = SYNC 1&2 1000 = SYNC 1&2 – rising edge 1001 = SYNC 1&2 – falling edge 1010 = READ INTERNAL REGISTER (single) 1011 = WRITE INTERNAL REGISTER (single) 1100 = READ INTERNAL REGISTER (continous) (*) 1101 = WRITE INTERNAL REGISTER (continous) 1110 = I²C TRANSFER 1111 = I²C STATUS

Table 23: Opcodes

(*) Not to be used in broadcast

OPCODE-BASED DATA

PROCESS_DATA_x

The register PROCESS_DATA_x is controlled via the opcode and therefore does not contain a register address itself.

The meaning and length of the opcode complies with the selected mode of the IO_SEL_x register and other involved registers if applicable. The register can transmit 32-bit, 16-bit, and 8-bit data and optionally can be switched off entirely. It contains the data of the primary channels.

PROCESS_DATA_x (DI)	P	R - /
bit 6:0	0000000	
bit 7	Digital input after spike filter, optionally inverted	

Table 24: Process data primary channel in DI mode

PROCESS_DATA_x (DO/PWM)	P	RW - 0x00
bit 6:0	0000000	
bit 7 OUT	Output, depending on DO_SEL, optionally inverted: PUSH-PULL: Output bit LOW-SIDE: 0 = line low (driver active) HIGH-SIDE: 1 = line high (driver active)	
bit 7 IN(*)	Reading of the physical line: digital input after spike filter, optionally inverted	

Table 25: Process data primary channel in DO mode

(*) No overlapping since there are different byes when writing and reading back.

PROCESS_DATA_x (VI/CI)	P	R - /
bit 15:0	Analog input value, see Tab. 5	

Table 26: Process data primary channel in VI/CI mode

PROCESS_DATA_x (VO/CO)	P	W - 0x0000
bit 1:0	Unused	
bit 15:2	Analog output value, see Tab. 7	

Table 27: Process data primary channel in VO/CO mode

PROCESS_DATA_x (CNT)	P	R(*) - 0x0000 0000
bit 31:0	Counter value (1 LSB = 125 ns)	

Table 28: Process data primary channel in CNT mode

(*) Setting of the counter possible via register communication.

PROCESS_DATA_x (TM)	P	R - /
bit 15:0	Temperature, see Tab. 10	

Table 29: Process data primary channel in TM mode

CH_STAT_REG

The register CH_STAT_REG is controlled directly via the opcode and therefore does not contain a register address.

The states of both primary channels and other status bits are stored in this register. The states of the channels depend on the selected mode (IO_SEL_xP) and can be activated via the EN_CH_STAT_xP register. When reading, the bits are reset automatically.

Note that bit 2, 3, 4, 5, and 6 can only be (de-)activated together because they are controlled by the same bit of the EN_CH_STAT_xP register. They assume their status independently though. In the following tables this is marked by horizontal lines.

Figure 7 explains the connection between the registers CH_STAT, SPV_REG, IRQ_FLAG_REG, and their *enable registers*.

CH_STAT_REG	P+	R+RST - 0x0000
bit 6:0	CH_STAT_1P, see Table 31 to 37	
bit 7	CH_STAT_12S_SUM – Sum of CH_STAT_1S and CH_STAT_2S	
bit 14:8	CH_STAT_2P, see Table 31 to 37	
bit 15	SPV_REG_SUM – Sum of SPV_REG	

Table 30: Channel status register

CH_STAT_x (DI)	P	R+RST - 0000000
bit 0	Mapping of digital input to spike filter and optional invertion (*)	
bit 6	1 = Overcurrent UNx	

Table 31: CH_STAT_x in DI mode

(*) When bit ENDOSC_x is activated, the output of the comparator that is also available for SPI is mapped instead.

CH_STAT_x (DO / CNT(PWM))	P	R+RST - 0000000
bit 0	1 = Cable break (*)	
bit 1	1 = Channel overtemperature (***)	
bit 2	1 = Overcurrent IAx (**)	
bit 6	1 = Overcurrent UNx	

Table 32: CH_STAT_x in DO/PWM mode

(*) Cable break detection is based on the pull-up/pull-down currents according to Item No. B04/B12. A cable break will only be detected when the driver is inactive and the connected load cannot pull away the current, i.e. in the following operating conditions:

1) Low-side driver configured and switched off (i.e. output at '1').

2) High-side driver configured and switched off (i.e. output at '0').

The identification has a dead time of td(),ol, to also enable high-resistance loads to discharge the line.

(**) The status bit for overcurrent is activated when an active driver cannot saturate anymore. This condition can be long-lasting, provided that the overtemperature monitoring remains inactive.

(***) The channel overtemperature, as defined in *overtemperature behavior*, switches off the digital driver. When the restart temperature is underrun, the driver is activated automatically. Therefore the driver oscillates with a thermal time-constant.

CH_STAT_x (VI/CI/TM(TE))	P	R+RST - 0000000
bit 0	1 = lower range underrun	
bit 1	1 = upper range overrun	
bit 2	1 = lower limit underrun	
bit 3	1 = upper limit overrun	
bit 4	1 = cable break UPx/current underrun (CI at 4...20 mA only)	
bit 5	1 = cable break UIx	
bit 6	1 = overcurrent UNx	

Table 33: CH_STAT_x in mode VI/CI/TE

(*) The current underrun is only active during current measurement operation with a configured 4 to 20 mA range and monitors the digital value for falling below 0xFD00 ≙ 3.602 mA.

CH_STAT_x (TM(PT))	P	R+RST - 0000000
bit 0	1 = lower range underrun	
bit 1	1 = upper range overrun	
bit 2	1 = lower limit underrun	
bit 3	1 = upper limit overrun	
bit 4	1 = cable break UPx (4-wire only)/cable break IA (2/3/4-wire)	
bit 5	1 = cable break UIx (3/4-wire only)	
bit 6	1 = overcurrent UNx	

Table 34: CH_STAT_x in mode TM(PT)

CH_STAT_x (VO)	P	R+RST - 0000000
bit 0	1 = overcurrent UPx (pin higher than nominal)	
bit 1	1 = overcurrent UPx (pin lower than nominal)	
bit 6	1 = overcurrent UNx	

Table 35: CH_STAT_x in mode VO

CH_STAT_x (CO)	P	R+RST - 0000000
bit 0	1 = cable break/R_load(*) IAx	
bit 6	1 = overcurrent UNx	

Table 36: CH_STAT_x in mode CO

(*) This bit is set if the cable at the relevant pin is broken or the combination of load resistance and current prevents the driver from saturatiing.

CH_STAT_x (CNT except PWM)	P	R+RST - 0000000
bit 0	Mapping of digital input to spike filter and optional inversion (*)	
bit 1	1 = counter underrun	
bit 2	1 = counter overrun	
bit 4	1 = counter reached reference value	
bit 5	1 = counter reached reference value #2 (CH_1 only, see bit CNT_E2R)	
bit 6	1 = overcurrent UNx	

Table 37: CH_STAT_x in mode CNT

(*) When bit ENDOSC_x is activated, the output of the comparator that is also available for the counter is mapped instead.

IRQ_FLAG_REG
The register IRQ_FLAG_REG is controlled directly via the opcode and therefore does not contain a register address.

The bits of the CH_STAT_REG register that were activated via EN_IRQ_FLAG_REG are mapped to this register. IRQ_FLAG_REG is no register as such. It is gen-

erated combinatorial and therefore can neither be written nor reset. To clear these bits, either CH_STAT_REG must be read whereby set bits are reset or the detection must be deactivated in EN_IRQ_FLAG_REG. Figure 7 shows the connection between the registers CH_STAT, SPV and IRQ_FLAGS.

IRQ_FLAG_REG	/	R - NA
bit 6:0	Active interrupts of CH_STAT_REG_1P	
bit 7	Sum of active interrupts of CH_STAT_REG_1S and CH_STAT_REG_2S	
bit 14:8	Active interrupts of CH_STAT_REG_2P	
bit 15	Sum of activen interrupts of SPV_REG	

Table 38: IRQ-Flag-Register

REGISTER MAP								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration channel 1								
0x00	ENVIF_1	IO_SEL_1S(2:0)			DO_12	IO_SEL_1P(2:0)		
0x01	SYNC_INV_1	SYNC_SEL_1(1:0)		DIO_INV_1	DO_SEL_1(1:0)		DI_SEL_1(1:0)	
0x02	ENDOSC_1	CNT_E2R_1	VO_EC_1	CO_SEL_1(1:0)		VICI_SEL_1(2:0)		
0x03(A)	CNT_DUAL	CNT_SEL_1(2:0)			CNT_CBE_1	CNT_DNU_1	CNT_RAR_1	CNT_DCB_1
0x03(B)	CNT_DUAL	CNT_SEL_1(2:0)			(unused)	PWM_LAP_1	PWM_AZP_1	PWM_HS_1
0x03(C)				TM_SEL_1(4:0)				
0x04	AI_LOWER_1(15:8)							
0x05	AI_LOWER_1(7:0)							
0x06	AI_UPPER_1(15:8)							
0x07	AI_UPPER_1(7:0)							
0x08	EN_CH_STAT_1S(3:0)				EN_CH_STAT_1P(3:0)			
0x09	SPIKE_FIL_1(3:0)				DIG_FIL_1(3:0)			
Configuration channel 2								
0x10	ENVIF_2	IO_SEL_2S(2:0)			DO_ADR0_2	IO_SEL_2P(2:0)		
0x11	SYNC_INV_2	SYNC_SEL_2(1:0)		DIO_INV_2	DO_SEL_2(1:0)		DI_SEL_2(1:0)	
0x12	ENDOSC_2	(unused)	VO_EC_2	CO_SEL_2(1:0)		VICI_SEL_2(2:0)		
0x13(A)	(unused)	CNT_SEL_2(2:0)			CNT_CBE_2	CNT_DNU_2	CNT_RAR_2	CNT_DCB_2
0x13(B)	(unused)	CNT_SEL_2(2:0)			(unused)	(unused)	PWM_AZP_2	PWM_HS_2
0x13(C)				TM_SEL_2(4:0)				
0x14	AI_LOWER_2(15:8)							
0x15	AI_LOWER_2(7:0)							
0x16	AI_UPPER_2(15:8)							
0x17	AI_UPPER_2(7:0)							
0x18	EN_CH_STAT_2S(3:0)				EN_CH_STAT_2P(3:0)			
0x19	SPIKE_FIL_2(3:0)				DIG_FIL_2(3:0)			
Digital filter setting								
0x1B	FIL_ITP_1	FIL_HB_1	FIL_ITP_2	FIL_HB_2				
SPV_INT								
0x1F					ST_VPD	ST_VPA	ST_VBG	ST_PLL

REGISTER MAP								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Counter								
0x20	SET_CNT_1(31:24)							
0x21	SET_CNT_1(23:16)							
0x22	SET_CNT_1(15:8)							
0x23	SET_CNT_1(7:0)							
0x24	SET_CNT_2(31:24)							
0x25	SET_CNT_2(23:16)							
0x26	SET_CNT_2(15:8)							
0x27	SET_CNT_2(7:0)							
0x28	REF_CNT_1(31:24)							
0x29	REF_CNT_1(23:16)							
0x2A	REF_CNT_1(15:8)							
0x2B	REF_CNT_1(7:0)							
0x2C	REF_CNT_2(31:24)							
0x2D	REF_CNT_2(23:16)							
0x2E	REF_CNT_2(15:8)							
0x2F	REF_CNT_2(7:0)							
General configuration								
0x30	SEL_ETK	VDA_VB	EN_SS	DIS_CAL	DIS_SPI2	DIS_SPI1	EN_SPI_WD	EN_UCM
EN_SPV_IRQ								
0x31	EN_CALIB	EN_CONF	EN_CT2	EN_CT1	EN_BIAS	EN_VDA	EN_VNB	EN_VB
Interrupt enable								
0x32	EN_IRQ_FLAG_REG(15:8)							
0x33	EN_IRQ_FLAG_REG(7:0)							
Secondary channel data								
0x34	DATA_1S(15:8)							
0x35	DATA_1S(7:0)							
0x36	DATA_2S(15:8)							
0x37	DATA_2S(7:0)							
Watchdog								
0x38	WATCHDOG(7:0)							
SPI_LOCK, software reset								
0x39	SPI_LOCK_RESET(7:0)							
Cold-junction temperature								
0x3A	TEMP_KSK(15:8)							
0x3B	TEMP_KSK(7:0)							
Chip temperature								
0x3C	CHIP_TEMP(7:0)							
Diagnostics measurements								
0x3D				EN_DIAG	DIAG_SEL_CH(3:0)			
0x3E	DIAG(13:6)							
0x3F	DIAG(5:0)							
Write EEPROM configuration								
0x40	WR_EEPROM_CONF(7:0)							

REGISTER MAP								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2C communikation								
0x41	I^2C_DEV_ADR(7:0)							
0x42	I^2C_PTR(7:0)							
0x43	I^2C_MODE(7:4)				I^2C_BYTES(3:0)			
0x44	I^2C_DATA_B1(7:0)							
0x45	I^2C_DATA_B2(7:0)							
0x46	I^2C_DATA_B3(7:0)							
0x47	I^2C_DATA_B4(7:0)							
ASIC revision & identification								
0x48	REV(7:0)							
0x49	CHARGE(7:0)							
0x4A	WAFER(4:0)					CHIP(10:8)		
0x4B	CHIP(7:0)							
Secondary channel status register								
0x4E		CH_STAT_1S(6:0)						
0x4F		CH_STAT_2S(6:0)						
SPV_REG								
0x52	ST_CALIB	ST_CONF	ST_CT2	ST_CT1	ST_BIAS	ST_VDA	ST_VNB	ST_VB

Table 39: Register layout

REGISTER DESCRIPTION

Unless otherwise noted, a '1' activates and a '0' deactivates a function. Registers with the suffix **_x** refer to both channel 1 and 2. Their function is the same but the channels can be configured independently.

The right hand side of the register header contains the following values:

'L': Shows that the register can be locked, see register SPI_LOCK_RESET.

'K': Marks those configuration registers which values are read from the external EEPROM during start-up.

'P', **'S'**: Represent the primary or secondary mode. Some registers refer to both modes and carry both letters, others are independent of the modes and carry **'/'** instead.

'R', **'W'**: Represents the access modes 'read' and 'write'.

'(*)': Represents the possibility of automatic configuration. Here, the iC autonomously selects the data content when required.

Finally, the default value that the register takes up after start-up is given. In configuration registers, this value is overwritten with the value of the EEPROM, if the register contains a configuration with a valid CRC value.

IO_SEL_xP, IO_SEL_xS, DO_ADR0_2
The primary and secondary mode for each channel can be selected via the registers IO_SEL_xP and IO_SEL_xS. For the secondary mode, digital voltage and current in- and outputs are available. For the primary mode, in addition, a counter that optionally can function as PWM generator and a temperature measurement is available. Chapter 'Mixed operation' shows possible combinations.

The exact function of the selected modes can be set by the relevant registers.

If the temperature measurement is selected in register IO_SEL_xP and the PT elements are selected in register TM_SEL_x, the register IO_SEL_xS is automatically overwritten with the selection CO to provide the current required for the measurement.

IO_SEL_xP	LK - P	RW - 011
000	DI – digital input	
001	DO – digital output	
010	VI – voltage input	
011	VO – voltage output	
100	CI – current input	
101	CO – current output	
110	CNT – counter, corresponds to DI when counting and DO for PWM	
111	TM – temperature mesurement	

Table 40: Primary channel mode selection

IO_SEL_xS	LK - S	(*) RW - 000
000	DI – digital input	
001	DO – digital output	
010	VI – voltage input	
011	VO – voltage output	
100	CI – current input	
101	CO – current output	
110	CNT(PWM) – counter in PWM mode, corresponds to DO; counter not supported	
111	OFF – NOP	

Table 41: Secondary channel mode selection

DO_12
The register DO_12 enables outputting a digital data signal for both channels. For control, any source of the first channel can be used. The output occurs simultaneously at both outputs. If the signals are output in phase (i.e. DIO_INV_1 = DIO_INV_2), the outputs can be connected in parallel and the maximum available current can thus be doubled. The antivalent operation for example is useful for differential mode generation via PWM.

DO_12	LK - P	RW - 0
1	Activates the output of a signal via DO_1 and DO_2	

Table 42: DO_12

DO_ADR0_2
Register DO_ADR0_2 enables outputting the input value at pin ADR0 directly at the digital output pin IA2. The possibility for inversion remains.

DO_ADR0_2	LK - P	RW - 0
1	Activates pin ADR0 → IA2	

Table 43: DO_ADR0_2

ENVIF_x
Register ENVIF_x enables the use of floating sensors when using the current and voltage input as well as thermocouples. If this bit is set, the pin UIx is switched to ground by means of a resistor.

ENVIF_x	LK-PS	RW - 0
1	Switches pin UI to ground – use with floating sensors	

Table 44: ENVIF_x

DI_SEL_x
Register DI_SEL_x allows selecting the digital input as type 1/2/3 in accordance with the standard DIN/EN 61131-2.

DI_SEL_x	LK-PS	RW - 11
00	Pull-up	
01	Type 1	
10	Type 2	
11	Type 3	

Table 45: Digital input selection

DO_SEL_x
Register DO_SEL_x enables to select the mode for the digital output. In push-pull mode, either the P-channel or the N-channel transistor is active to pull the output actively to the appropriate level. In low-side mode, only the N-channel transistor and a small pull-down current-source for cable break detection are active. Correspondingly, in high-side mode, only the P-channel transistor and a small pull-up current are active.

DO_SEL_x	LK-PS	RW - 00
00	Push-pull	
01	IO-Link with push-pull	
10	Low-side driver	
11	High-side driver	

Table 46: Digital input/output selection

DIO_INV_x
The input and output signals can be inverted with the DIO_INV_x register. At the input, all modes are affected that use the digital input, i.e. also counters and the read-back of the physical line level. At the output, all modes are affected that use the digital output, i.e. the counter in PWM mode.

DIO_INV_x	LK-PS	RW - 0
0	OFF – input/output not inverted	
1	ON – input/output inverted	

Table 47: Digital input/output inversion

SYNC_SEL_x
According to table 48, both SYNC pins can be operated separately in the following modes. Note that for modes

that use the digital input or output, those in- and outputs must also be selected in the IO_SEL_xX register – either as primary or secondary function.

- **OUT:** The iC operates asynchronously. The input data is sampled with the falling edge at pin NCS (SPI access), the output data is set after writing (rising edge at NCS; the analog outputs are updated after the next refresh cycle).
- **SYNC (DATA):** The iC operates synchronously. The input data is sampled with the rising or falling edge of the SYNC pin and can be read via SPI at any time. The output data written via SPI is output then (the analog outputs are updated after the next refresh cycle).
- **DIG_IN-SYNC_OUT:** The digital input data is output via the SYNC pin after passing the spike filter and optional inversion. The mode of the digital input is selected via DI_SEL. The primary or secondary function for the channel must be selected as DI.
- **SYNC_IN-DIG_OUT:** The digital value at the SYNC pin is output (optionally inverted) at the digital output. The mode of the digital output is selected via DO_SEL. The primary or secondary function for the channel must be selected as DO.

SYNC_SEL_x	LK - /	RW - 00
00	OFF	
01	SYNC (DATA)	
10	DI → SYNC_PIN	
11	SYNC_PIN → DO	

Table 48: SYNC pin function selection

SYNC_INV_x
The register SYNC_INV_x selects the active edge for synchronizing (for every channel separately). This applies both to the SYNC pin and the SYNC command via SPI.

SYNC_INV_x	LK - P	RW - 0
0	Non inverted: rising edge	
1	Inverted: falling edge	

Table 49: SYNC edge selection

VICI_SEL_x
Register VICI_SEL_x determines the function of the voltage input or the current input respectively. The setting must correspond to register IO_SEL_x.

When temperature measurement is selected in register IO_SEL_xP, it is automatically overwritten with the voltage range required for the measurement.

VICI_SEL_x	LK-PS	(*) RW - 000
000	±10 V	
001	±1 V	
010	±100 mV	
011	±10 mV	
100	-17.5m...87.5 mV	
101	-4.375...21.875 mV	
110	-20...20 mA	
111	4...20 mA	

Table 50: Voltage/current input selection

CO_SEL_x
Register CO_SEL_x determines the function of the current output.

When temperature measurement is selected in register IO_SEL_xP and the PT elements are selected in register TM_SEL_x, this register is automatically overwritten with the selection appropriate for the PT elements to supply the required current.

CO_SEL_x	LK-PS	(*) RW - 00
00	0...20 mA	
01	4...20 mA	
10	0...2.0 mA	
11	0...200 µA	

Table 51: Current-output selection

VO_EC_x
Register VO_EC_x activates the extended current range of the voltage output (see Item No. M04).

VO_EC_x	LK-PS	(*) RW - 0
1	Activates the extended current range of VO	

Table 52: Current-range extension

Classic counter
The following registers refer to the function of the counter in *classic* mode. This register block shares its functions with other modes. It is only valid, if the *classic* counter is selected in register IO_SEL_xP.

If required, register CNT_DCB_x suppresses several CH_STAT events in consequence of the same trigger. They can be reactivated in register SPI_LOCK_RESET. The bit is intended to reduce double interrupts due to a single event.

CNT_DCB_x	LK - P	RW - 0
1	Activates the suppression of multiple CH_STAT events	

Table 53: EN_STAT_xP-bits reset

Register CNT_RAR_x resets the counter when reaching the reference value. The reference value as such is not reached.

CNT_RAR_x	LK - P	RW - 0
1	Activates the counter reset when the reference value is reached	

Table 54: Reset at reference

Register CNT_DNU_x enables switching the counting direction. This function is supported by the following modes:

- Single: Pulse counter
- Dual: Pulse counter with trigger
- Dual: Pulse counter with reset
- Dual: Pulse counter with gate

CNT_DNU_x	LK - P	RW - 0
0	up (where available)	
1	down (where available)	

Table 55: Counting direction

Register CNT_CBE_x is relevant for all counter modes that count pulses, both in single and dual mode. It enables selecting whether only one type of edge (rising or falling) or both are counted. In the first case, the edge is selected via register DIO_INV_x.

CNT_CBE_x	LK - P	RW - 0
0	Only one type of edge is counted (rising or falling, cf. DIO_INV_x)	
1	Both edges are counted (rising and falling)	

Table 56: Edges

Register CNT_E2R_1 is implemented only for the first channel. The first counter can be compared with both reference values and the equality is indicated via the respective status bit. This is possible both in single and in dual mode. The possibility to prevent several interrupts via register CNT_DCB_1 remains for both comparisons separately.

This mode is not possible if the second counter is in PWM mode, since the reference register is required there. The second counter can be operated as a classic counter, with the restriction that its reference register can be used twice but can only have one value. The second channel can carry out every function without restriction.

CNT_E2R_1	LK - P	RW - 0
1	Additionally acatives the comparison of the first counter with a second reference value	

Table 57: Second reference

CNT_SEL_x in single-Mode	LK - P	RW - 000
000	Pulse counter	
001	Time measurement period	
010	Time measurement pulse width	
011	PWM (output)	

Table 58: Mode selection in single-mode

CNT_SEL_x in dual-mode	LK - P	RW - 000
000	Pulse counter with trigger	
001	Pulse counter with reset	
010	Pulse counter with gate	
011	Pulse counter with direction signal	
100	Time-measurement edge between channel 1 and 2	
101	Incremental encoder single	
110	Incremental encoder dual	
111	Incremental encoder quadruple	

Table 59: Mode selection in dual-mode

CNT_DUAL_1	LK - P	RW - 0
1	Activates the dual-mode: both inputs combined control one counter; to be configured for channel 1; both channels must be configured as counters	

Table 60: Selection single-/dual-mode

Counter PWM

The following registers refer to the function of the counter in PWM mode. This register block shares its functions with other modes. It is only valid if the PWM counter is also selected in register IO_SEL_xP.

PWM_HS_x	LK - P	RW - 0
0	LOW-SPEED MODE, see Tab. 75	
1	HIGH-SPEED MODE, see Tab. 75	

Table 61: Selection low-speed/high-speed

Register PWM_AZP_x enables the activation pulse of the PWM. When switching on the PWM, a (usually) long activation pulse is generated before the PWM starts. An inversion at the input and output is still possible.

PWM_AZP_x	LK - P	RW - 0
1	PWM generates an activation pulse	

Table 62: PWM activation pulse

The bit PWM_LAP_1 (only present in the first channel) is intended for operation of the PWM in antivalent mode. If it is active and a channel is inverted in active mode (DO = '1'), both outputs operate in antivalent mode. In inactive mode, (DO = '0') both outputs are set to the same state depending on DIO_INV_1 and _2 either '0' or '1'. The use of this bit requires the bit DO_12.

PWM_LAP_1	LK - P	RW - 0
1	PWM_2 anitvalent or in phase with PWM_1 when off	

Table 63: PWM antivalent gating

TM_SEL_x
The following registers refer to the function of temperature measurement. This register block shares its functions with other modes. It is only valid if the temperature measurement is also selected in the IO_SEL_xP register.

The thermocouples do not require any further settings except the selection of the temperature measurement in register IO_SEL_x, i.e. the voltage measurement range is selected automatically by the iC. The same applies to the PT-temperature sensors, whereas, additionally, the required current must be set as secondary function, i.e. both registers CO_SEL_x and DATA_xS. The current must be selected in such a way that the nominal value i.e. at 0 °C results in a voltage of exactly 170 mV. Table 65 helps selecting appropriate output currents.

TM_SEL_x	LK - P	RW - 00000
00000	Thermo-couple J	
00001	Thermo-couple K	
00010	Thermo-couple T	
00011	Thermo-couple N	
00100	Thermo-couple E	
00101	Thermo-couple R	
00110	Thermo-couple S	
00111	Thermo-couple B	
11000	PT sensor, 2-wire	
11001	PT sensor, 3-wire	
11010	PT sensor, 4-wire	

Table 64: Temperature measurement selection

PT-Element	CO_SEL_x	DATA_xS
PT100	0...2 mA (10)	1.7 mA (0xCF3C)
PT200	0...2 mA (10)	0.85 mA (0x67A0)
PT300	0...2 mA (10)	0.5667 mA (0x4514)
PT500	0...2 mA (10)	0.34 mA (0x2974)
PT1000	0...200 µA (11)	170 µA (0xCF3C)
PT2000	0...200 µA (11)	85 µA (0x67A0)
PT3000	0...200 µA (11)	56.67 µA (0x4514)
PT5000	0...200 µA (11)	34 µA (0x2974)
PT9000	0...200 µA (11)	18.89 µA (0x1708)

Table 65: PT current selection examples

EN_CH_STAT_xX
Register EN_CH_STAT_xX activates the bits of register CH_STAT_xX. Note that bits 2, 3, 4, 5, and 6 can only be activated en masse. This is relevant for the limit detection. This limit can easily be restricted to just exceeding or falling below by setting the appropriate limit value to the maximum or minimum of the range. Figure 7 shows the connection between the registers CH_STAT, SPV and IRQ_FLAG_REG.

CH_STAT_xX	LK-PS	RW - 0x0
bit0	activates relevant CH_STAT_xX, bit 0	
bit1	activates relevant CH_STAT_xX, bit 1	
bit2	activates relevant CH_STAT_xX, bits 2, 3	
bit3	activates relevant CH_STAT_xX, bits 4, 5, 6	

Table 66: CH status

DIG_FIL_x
Via register DIG_FIL_x, the cut-off frequency of the digital filter can be set to filter the analog signals after the AD converter. The cut-off frequencies also depend on register FIL_HB_x.

DIG_FIL_x	LK-PS	RW - 0x0
	valid for FIL_HB_x = '0'	
0x0	2 kHz	
0x1	1 kHz	
0x2	500 Hz	
0x3	250 Hz	
0x4	125 Hz	
0x5	62.5 Hz	
0x6	31.2 Hz	
0x7	15.6 Hz	
0x8	7.8 Hz	
0x9	3.9 Hz	
0xA	1.9 Hz	
0xB	0.97 Hz	
0xC	0.50 Hz	
	valid for FIL_HB_x = '1'	
0x0	3.50 kHz (only with voltage measurement)	
0x1	1.75 kHz (only with voltage measurement)	
0x2	875 Hz	
0x3	440 Hz	
0x4	220 Hz	
0x5	110 Hz	
0x6	55 Hz	
0x7	27.5 Hz	
0x8	14 Hz	
0x9	7 Hz	
0xA	3.5 Hz	
0xB	1.75 Hz	
0xC	0.875 Hz	

Table 67: Digitale filter cut-off frequencies (rounded)

FIL_HB_x
Via register FIL_HB_x, the digital input filter for the analog signals can be switched into a faster mode with reduced latency but flatter amplitude response. This involves an internal deactivation of the half-band filters. See register 'DIG_FIL_x'.

FIL_HB	LK-PS	RW - 0
0	Steeper amplitude response with higher latency	
1	Flatter amplitude response with lower latency	

Table 68: FIL_HB_x

FIL_ITP_x
Via register FIL_ITP_x, the digital input filter for the analog signals can be switched into a faster mode with reduced latency but much lower sample rate. This involves a deactivation of the interpolation which results in about halving the latency.

FIL_ITP	LK-PS	RW - 0
0	Active interpolation with higher latency	
1	Deactive interpolation with lower latency	

Table 69: FIL_ITP_x

SPIKE_FIL_x
The digital spike filter can be set for every channel separately. It serves to filter the digital input for spurious pulses up to a configurable length.

The digital spike filter can be set via the 4-bit-wide register SPIKE_FIL_x in the range of 0 up to approx. 262 ms. To deactivate the filter, the time can be set to 0. Internally, the filter operates with an 8-bit counter. If the input is 0, the counter is counted down, if it is 1, it is counted up. If the counter reaches 0, the output is set to 0. If the counter achieves its maximum value dependent on the filter width, it is set to 1.

Table 70 summarizes the settings of SPIKE_FIL_x, the resulting filter time and in brackets the internal sample rate and filter width. The given times have an accuracy of ±1 clock. This is equal to an accuracy e.g. at 8 MHz sampling of ±125 ns.

SPIKE_FIL_x	LK-PS	RW - 0x7
0x0	0 µs ..... (8 MHz, spike-filter off)	
0x1	16 µs ..... (8 MHz, 7-bit counter)	
0x2	32 µs ..... (8 MHz, 8-bit counter)	
0x3	64 µs ..... (4 MHz, 8-bit counter)	
0x4	128 µs ..... (2 MHz, 8-bit counter)	
0x5	256 µs ..... (1 MHz, 8-bit counter)	
0x6	512 µs ..... (500 kHz, 8-bit counter)	
0x7	1.024 ms ..... (250 kHz, 8-bit counter)	
0x8	2.048 ms ..... (125 kHz, 8-bit counter)	
0x9	4.096 ms ..... (62.5 kHz, 8-bit counter)	
0xA	8.192 ms ..... (31.25 kHz, 8-bit counter)	
0xB	16.38 ms ..... (15.63 kHz, 8-bit counter)	
0xC	32.77 ms ..... (7.813 kHz, 8-bit counter)	
0xD	65.54 ms ..... (3.906 kHz, 8-bit counter)	
0xE	131.1 ms ..... (1.953 kHz, 8-bit counter)	
0xF	262.1 ms ..... (0.977 kHz, 8-bit counter)	

Table 70: Spike-filtertime setting

AI_LOWER_x, AI_UPPER_x
Registers AI_LOWER_x and AI_UPPER_x describe the valid range in which the analog input should stay. If the detection in the EN_CH_STAT_xX register is activated, a status bit indicates when this range is left. The status bit remains set until the status register is read to ensure that temporarily leaving the range will also be detected.

AI_LOWER_x	LK-PS	RW - 0x8000
bits 15:0	Lower limit (last valid value)	

Table 71: Lower limit

AI_UPPER_x	LK-PS	RW - 0x7FFF
bits 15:0	Upper limit (last valid value)	

Table 72: Upper limit

SPV_INT
Register SPV_INT monitors the internal status. In case of an error, the relevant bit is set to '1' and remains set until the register is read via SPI. The register is shown in figure 7. It is not linked to the others registers though.

SPV_INT	/	R - 0x00
ST_PLL	Status PLL	
ST_VBG	Status band-gap voltage VBG	
ST_VPA	Status internal supply voltage VDP	
ST_VPD	Status internal supply voltage VPD	

Table 73: Internal monitor bits status

SET_CNT_x
Register SET_CNT_x enables setting the particular counter to a specific value. Via the register communication, the register can be set both in single or continuous mode. When writing the last register byte, the written 16/32-bit-wide word is taken as a whole. In regular counter modes, only setting the register as a whole is useful. In PWM mode or with activation pulse mode, either the entire register or only the lower half (bits 15:0) can be set. Except for this, a partial writing of the register is not possible. The meaning of the register depends on the selected mode (see chapter 'Counter').

SET_CNT_x	P	W - 0x00000000
bits 31:0	Counter value	

Table 74: Set counter

REF_CNT_x
Register REF_CNT_x enables setting the counter reference value. Via the register communication, the register can be set both in single and in continuous mode. When writing on the last register byte, the written 16/32-bit-wide word is taken as a whole. It is possible to set the register as a whole (bits 31:0) or to set only the lower half (bits 15:0). In PWM mode, it is useful to set only the lower half (bits 15:0). Except for this, a partial writing of the register is not possible. The meaning of the register depends on the selected mode (see chapter 'Counter').

REF_CNT_x	P	RW - 0x00000000
Bits 31:0	Reference value	

Table 75: Set counter reference

Monitoring
The bits of the monitoring register signal errors of individual supply voltages and overtemperature. In case of an error, the relevant bit is set to '1' and remains set until the register is read out via the SPI. This enables to detect voltage dips that occurred temporarily.

SPV_REG	/	R - 0x00
ST_VB	Supply voltage VB	
ST_VNB	Supply voltage VNB	
ST_VDA	Supply voltage VDA	
ST_BIAS	Bias (RREF)	
ST_CT1	Chip temperature 1 (cf. Toff1)	
ST_CT2	Chip temperature 2 (cf. Toff2)	
ST_CONF	Configuration (CRC error)	
ST_CALIB	Configuration (CRC error)	

Table 76: Supervisory bits

EN_SPV_IRQ	LK - /	RW - 0x00
EN_VB	VB monitor activation	
EN_VNB	VNB monitor activation	
EN_VDA	VDA monitor activation	
EN_BIAS	Bias monitor activation	
EN_CT1	CT1 monitor activation	
EN_CT2	CT2 monitor activation	
EN_CONF	Configuration monitor activation	
EN_CALIB	Configuration monitor activation	

Table 77: Supervisory bits activation

EN_IRQ_FLAG_REG
The bits in register EN_IRQ_FLAG_REG activate the relevant bits in register IRQ_FLAG individually.

EN_IRQ_FLAG_REG	LK - /	RW - 0x0000
bit 15:0	Activates individual bits of register IRQ_FLAG_REG(15:0)	

Table 78: IRQ flag activation

DATA_xS
Registers DATA_xS contain data of the secondary channel. If the secondary channel operates as input, the current values of the secondary channel can be read. If the secondary channel operates as output, output data can be written to the register. The communication proceeds via the regular register communication in single or continuous mode.

Applying for modes using 16-bit wide values:

When the data is read, the lower half of the register word is latched to ensure that a valid word is read out. When the data is written, the word is assumed as a whole only after transmission of the lower half.

Applying for modes using 8 bit wide values:

The values must be written or read left-aligned, i.e. only the bits 15:8 are used.

Usually, data is formatted identically to the data of the primary channels.

DATA_xS	S	(*) RW - 0x0000
	Secondary channel data (in/out)	

Table 79: Secondary channel data

EN_UCM
Via register EN_UCM, SPI communication can be selected between FPGA and µC mode. In FPGA mode, the bit is '0' for all iCs. In µC mode, the bit is '0' for all iCs except the last iC which must be '1'.

EN_UCM	LK - /	RW - 0
0	FPGA modus: no additional delay	
1	µC mode: additional clocks	

Table 80: µC mode

EN_SPI_WD
Register EN_SPI_WD activates the watchdog which is used for SPI communication. If the watchdog is active and no valid SPI communication takes place during a determined period, the watchdog resets the chip. Details can be found in chapter 'Startup, reset, watchdogs, and EEPROM'.

EN_SPI_WD	LK - /	RW - 0
0	SPI watchdog inactive	
1	SPI watchdog active	

Table 81: SPI watchdog

DIS_SPI_x
When required, register DIS_SPI_x deactivates the process data of the SPI communication for channel x. This bit affects only the opcodes "Process Data 1/2/1&2". If a channel is not used, it does not require time by setting this bit during the SPI communication. An interesting use is in broadcast operation with chains of iCs with partially unused channels.

DIS_SPI_x	LK - P	RW - 0
0	Channel x active	
1	Channel x inactive	

Table 82: Disable SPI CH_x

DIS_CAL
When required, register DIS_CAL deactivates the calibration of the chip. This register is checked only when the chip starts up, therefore its state must be stored in the EEPROM.

DIS_CAL	LK-PS	RW - 0
0	Calibration active	
1	Calibration inactive	

Table 83: Disable channel calibration

EN_SS
When required, register EN_SS activates the spectrum spread of the internal oscillator.

EN_SS	LK - /	RW - 0
0	Spread spectrum inactive	
1	Spread spectrum active	

Table 84: Enable spread spectrum

VDA_VB
When the digital output is not used, register VDA_VB enables to omit the 24 V digital supply voltage. Instead, the analog voltage VB can be connected to the pin VDA. In this case this bit should be set to adapt the internal voltage monitoring accordingly.

VDA_VB	LK - /	RW - 0
0	VDA = 24 V, digital output used	
1	VDA = VB, digital output not used	

Table 85: VDA at VB

SEL_ETK
Register SEL_ETK selects the calibration values that are used for the TK compensation and chip-temperature calibration (ATK, AITK, and AOCT). These can either be taken from the internal chip, if they were specified in the chip production process, or they can be taken from the external EEPROM where they can be specified subsequently. Independent of their use, the values that are stored in the EEPROM are used for the calculation of the CRC value.

SEL_ETK	LK - /	RW - 0
0	Internal calibration values are used	
1	External calibration values are used	

Table 86: SEL_ETK

SPI_LOCK_RESET
Register SPI_LOCK_RESET is not a classical register. It possesses multiple functions that can be activated by writing *keywords*: When writing 0xCA, a software reset is triggered – the chip restarts. When writing 0xA5, the SPI access for all registers is enabled in accordance with the register overview. Writing 0x00 (and further bytes) disables writing access of the SPI to the configuration registers marked with 'L'. After configuration, this helps to prevent accidental writing on the configuration registers in regular operation.

When writing 0xC5, the counter enables a one-shot CH_STAT event (prevention of multiple interrupts at one event). This only affects the counter if the bit CNT_DCB is set.

Writing with 0xAA activates a special calibration mode where registers that are usually inaccessible are additionally unlocked. In this process, the usually active address translation is switched off so that some registers change their addresses. This function should only be activated during calibration and only according to the extent described in chapter 'Calibration'.

When reading, this register returns four bits of status information. These bits are reset by read access (RD+RST). The first status bit is set if an illegal read access occured. The second status bit is set if an illegal write access occured. This relates both to locked registers and the access of non-existing addresses.

Note that a prefetching proceeds in mode READ_REG_CONTINOUS. As a result, illegal read accesses that already occur internally may be indicated without being deliberately controlled by the SPI. The third status bit indicates the condition of the lock.

(*) The initial state of this 'register' depends on the validity of the configuration data. If a valid configuration is stored in the EEPROM, the SPI is locked after starting up the chip. If the configuration is invalid, the SPI is not locked.

SPI_LOCK_RESET	/	RW+RST - (*)
bit 0 read	Status illegal read, 1 = detected	
bit 1 read	Status illegal write, 1 = detected	
bit 2 read	Status lock, 1 = locked	
bit 3 read	Status calibration mode, 1 = active	
bit 7:4 read	0000	
0xCA write	Software reset	
0xA5 write	Configuration register write enabled	
0xC5 write	CNT_STAT_REARM: signle CH_STAT counter event enabled (*)	
0xAA write	Calibration mode enabled. Caution! Further parts of the register map become invalid, see section 'Calibration'.	
0x00 write	Configuration register write disabled	

Table 87: SPI lock/reset

(*) Unlocking refers to the following 4 states: overflow, underflow, REF_1 reached, REF_2 reached.

TEMP_KSK
Register TEMP_KSK contains the cold junction temperature that is necessary for the thermocouple measurement. The register can be written both in single and continuous mode. It accepts its value internally only when the writing process of the second half is completed so that a consistent value is processed. It can only be written to as a whole.

TEMP_KSK	P	RW - 0x0BA6 (≙25°C)
bits 15:0	Cold-position temperature, 0x0000 ≙ 0K, 1 LSB ≙ 0.1 K	

Table 88: Cold-position temperature

CHIP_TEMP

CHIP_TEMP	/	R - /
bits 7:0	Chip temperature, 0x00 ≙ -64 °C, 1 LSB ≙ 1 °C	

Table 89: Chip temperature

EN_DIAG
Register EN_DIAG activates the diagnostic measurement. The channel for analysis is selected via register DIAG_SEL_CH. The result is continuously updated in register DIAG_CH with an update frequency in accordance with the analog output. The first valid measurement value must be waited for accordingly.

EN_DIAG	/	RW - 0
1	Diagnostic modus active	

Table 90: Diagnostics channel selection

DIAG_SEL_CH

DIAG_SEL_CH	/	RW - 0000
0000	VB	
0001	VNB	
0010	VCC	
0011	VDA	
0100	VPA	
0101	VPD	
0110	VI	
0111	V020	
1000	V420	
1001	Channel 1: Digital output current	
1010	Channel 2: Digital output current	

Table 91: Diagnostics selection

DIAG_CH	/	R - /
	see Tab. 12	

Table 92: Diagnostics channel

WR_EEPROM_CONF

Register WR_EEPROM_CONF stores the current configuration. After writing 0x96 to this register, the chip automatically writes the current configuration, i.e. all registers marked with 'K', to the EEPROM. Subsequently, also the valid CRC checksum is written. When the writing process is completed, the register is set; 0 signifies error-free writing, 1 signifies an error. This register can be polled for the end of the writing process.

WR_EEPROM_CONF	L - /	RW - 0x00
0x96 write	Starts write	
0x96 read	Write in progress	
0x00 read	Last write succesfull	
0x01 read	Last write failed	

Table 93: Write configuration

I²C

The chip contains an I²C interface. An external EEPROM must be connected to it which contains the configuration and calibration data required for operation. Additionally, it enables accessing other chips in the form of a bridge between SPI and I²C. For example temperature sensors with I²C interface can be controlled and their temperature data can be written via SPI on the registers of the cold junction compensation.

The currently valid configuration data can be transmitted automatically to the EEPROM via register WR_EEPROM_CONF. The calibration data must be written to the EEPROM in bridge mode and the matching checksums must be transmitted.

In all cases, the chip operates as an I²C master at up to 100 kbit/s. The interface is not capable of multi-master operation. The 7-bit addressing mode is supported. Note that an EEPROM with a page size of at least 2 bytes is required for operation. When writing several bytes to EEPROM it must be additionally ensured that the page limit is not exceeded. More information can be found in the relevant datasheet.

The following registers are of importance to use the bridge:

- I2C_DEV_ADR: This register contains the address of the chips to be addressed, e.g. 0xA0 for EEPROMs
- I2C_PTR: This register operates as pointer. It addresses a particular register at the addressed chip.
- I2C_MODE: According to table 96, it can be selected between the modes RD; RD[PTR], and WR[PTR].
- I2C_BYTES: This register indicates the number of bytes that are to be read or written. Values between 1 and 4 are valid.
- I2C_DATA_Bx: During the writing process, the bytes stored here are written; during read process the bytes that are read are stored here.

Except for the data bytes, no I²C register is changed during I²C communication. A valid setting can be maintained for an infinite time. If the registers are set correctly, the communication can be started via opcode I²C-TRANSFER. Opcode I²C Status can be polled for its end. Note that after successful writing accesses, EEPROMs require time for the internal writing. Within this time-window it does not respond to requests. When writing, a waiting period in accordance with the EEPROM specification is to be maintained.

I2C_DEV_ADR	/	RW - undef
	Chip address	

Table 94: I²C device address

I2C_PTR	/	RW - undef
	Pointer to address the chip	

Table 95: I²C pointer

I2C_MODE	/	RW - undef
0x1	RD: Read from current address	
0x2	RD[PTR]: Write from [PTR]	
0x4	WR[PTR]: Read from [PTR]	

Table 96: I²C mode

I2C_DATA_Bx	/	RW - undef
	Data bytes for I²C communikation	

Table 97: I²C data bytes

Feedback opcode I²C status	/	R - undef
0x00	Communication ended successful	
0x01	Communication running	
0x03	Communication failed	

Table 98: Opcode I²C status

Revision and identification

Register REV contains the hardware revision number of the iC, beginning with 1. The registers LOT, WAFER and CHIP set up a unique identification number defined during chip production.

REV	/	R - /
bits 7:0	Hardware revision number	

Table 99: Revision number

LOT	/	R - /
bits 7:0	Lot number	

Table 100: Lot number

WAFER	/	R - /
bits 4:0	Wafer number	

Table 101: Wafer number

CHIP	/	R - /
bits 10:0	Chip number	

Table 102: Chip number

WATCHDOG

Register WATCHDOG provides information on the cause of the last reset. If all bits are 0, the iC restarted because of a power-on reset. Otherwise, exactly one bit is set according to table 103. Details can be found in chapter 'Startup, Reset, Watchdogs, and EEPROM'.

WATCHDOG	/	R - 0x0
bit 0	NRES pin	
bit 1	SW reset	
bit 2	SPI watchdog	
bit 3	µP watchdog	

Table 103: Watchdog

CH_STAT_xS

Register CH_STAT_xS contains the status bits of the secondary channel. The meaning of the bits depends on the selected mode IO_SEL_xS. The meaning is identical with the meaning of the primary channel.

CH_STAT_xS	S	R - 0000000
bits 6:0	see Tab. 31 to 37	

Table 104: Secondary channel status register

ORDERING INFORMATION

Type	Package	Order Designation
iC-GD	QFN38 5 mm x 7 mm	iC-GD QFN38-5x7

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