iC-LA
64X1 LINEAR IMAGE SENSOR

iC-Haus

FEATURES

- 64 photosensors with 200 µm pitch and an active area of 0.037 mm^2 (ca. 183 µm x 200 µm)
- Integrating amplifiers and track-and-hold feature
- Low image lag
- Integration time can be set externally
- Internal bi-directional shift register
- Extendable data I/O supports multiple sensor operation
- On-chip temperature sensor
- Detection of low supply voltage
- TTL-/CMOS-compatible logic inputs and outputs
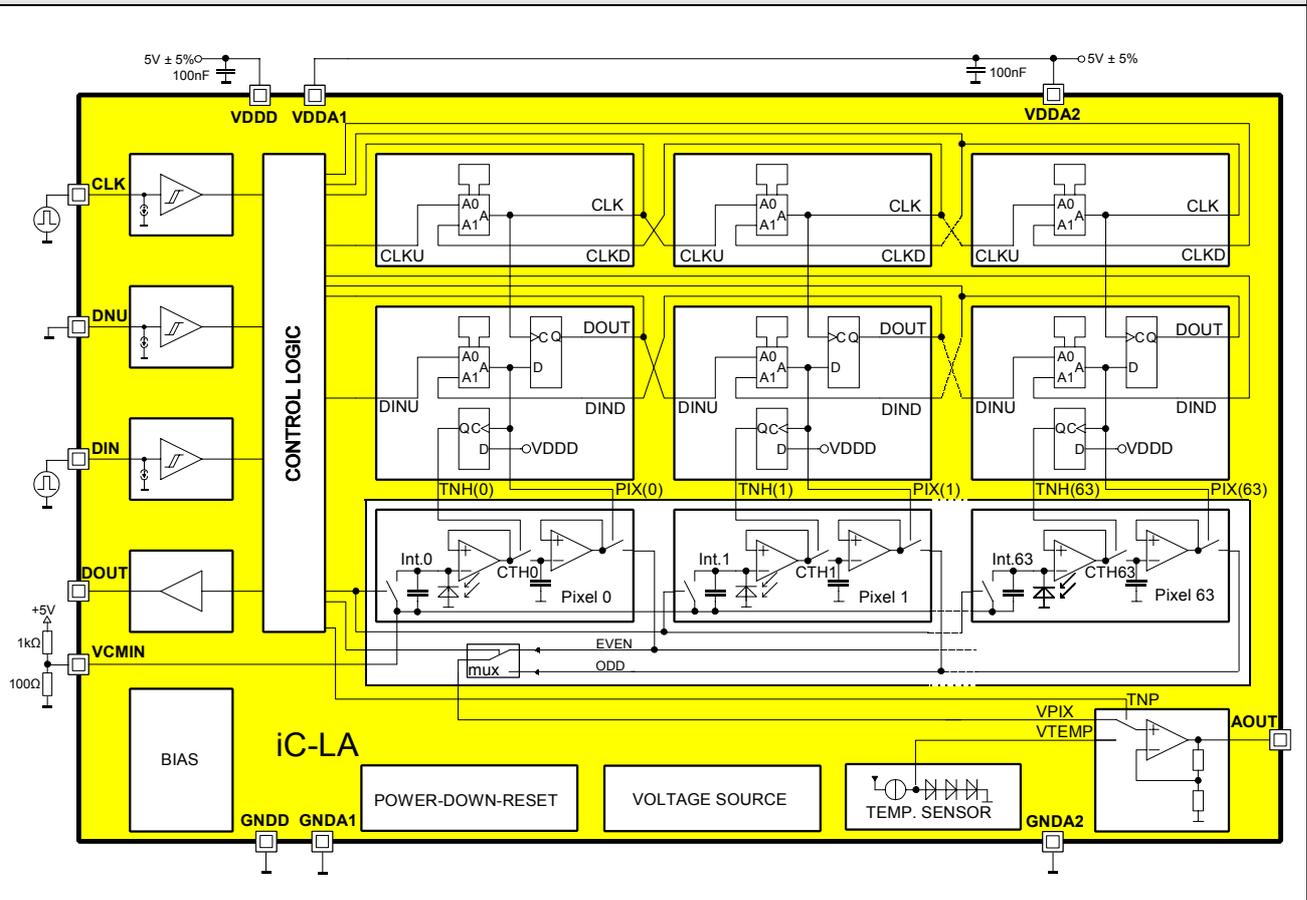- Single 5 V operation, separate analog supply

APPLICATIONS

- Optical linear sensors
- CCD substitute

CHIP

13.0 mm × 2.0 mm

BLOCK DIAGRAM

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DESCRIPTION

iC-LA is an integrating light-to-voltage converter with a row of 64 separate pixels. Each pixel consists of one photodiode, an integration capacitor and a track-and-hold circuit. For each pixel the photocurrent of the photodiode charges the integration capacitor. The track-and-hold circuit reads out the capacitor voltage in track mode; when the circuit switches into hold mode this voltage is present for one clock cycle at output AOUT.

Photocurrent integration is started simultaneously for all pixels with the rising edge of the clock signal if DIN has received a high signal. Following hold mode, the pixels are subsequently selected by their output switches. The downstream multiplexer selects the odd or even bus line for the output buffer. This dual line configuration means that a high working speed is obtained.

The switches are controlled by the shift register whereas the multiplexer is operated by the control logic. The DNU input signal determines the direction of shift. If DNU is low, the pixel signals are switched in ascending order to AOUT, starting at pixel 0. If DNU is high, the pixels are switched in descending order, starting at pixel 63.

If input DIN is still high at the end of a completed integration cycle, all integration capacitors are automatically reset and a new integration cycle is initiated. Continuous operation of the iC is thus possible.

All registers are reset with low voltage at the digital supply (power-down reset). All pins are protected against damage by ESD.

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CHIP LAYOUT

dimensions in µm; chip size 2.0 mm × 13.0 mm

PAD DESCRIPTION

Name	Function
VDDA2	+5 V Analog Supply Voltage 2
AOUT	Analog Output
GNDA2	Analog Ground 2
VCMIN	Offset Voltage Input for integration capacitor (connection to GNDA1, GNDA2 possible)
CLK	Clock Input
DNU	Down-Not-Up Input (pixel order is 0 to 63 when lo)
DIN	Data Input
DOUT	Data Output
VDDD	+5 V Digital Supply Voltage
GNDD	Digital Ground
GNDA1	Analog Ground 1
VDDA1	+5 V Analog Supply Voltage 1

External connections of VDDA1, VDDA2, VDDD to +5 V and GNDA1, GNDA2, GNDD to 0 V are required.

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item Nr.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VDDA	Analog Supply Voltage			-0.3	6	V
G002	VDDD	Digital Supply Voltage			-0.3	6	V
G003	I(VDDA)	Current in VDDA			-25	25	mA
G004	I(VDDD)	Current in VDDD			-25	25	mA
G005	V()	Voltage at pins AOUT, VCMIN, CLK, DNU, DIN, DOUT			-0.3	VDDA + 0.3	V
G006	I()	Current in pins AOUT, VCMIN, CLK, DNU, DIN, DOUT			-10	10	mA
E001	Vd()	ESD Susceptibility at all pins	MIL-STD-883, method 3015 HBM 100 pF discharged over 1.5 kΩ			2	kV
TG1	Tj	Junction Temperature			-25	90	°C
TG2	Ts	Storage Temperature	see package specification				

THERMAL DATA

Operating Conditions: VDDA(1,2) = VDDD = 5 V ±5%, GNDA(1,2) = GNDD = 0 V

Item Nr.	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range	see package specification					°C

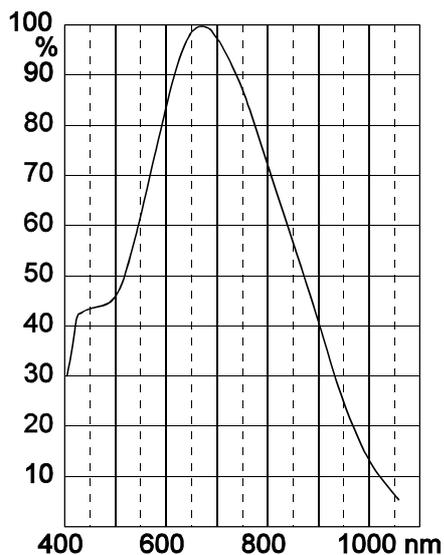## ELECTRICAL and OPTICAL CHARACTERISTICS: Diagrams

Fig. 1: typical relative spectral sensitivity, chip (bandwidth 30 nm)
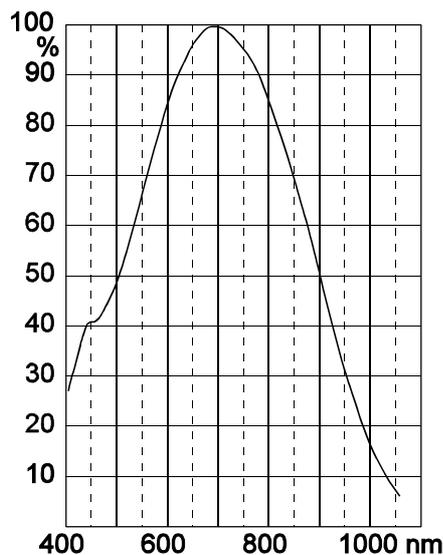

Fig. 2: typical relative spectral sensitivity with BMST assembly (bandwidth 30 nm)

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ELECTRICAL and OPTICAL CHARACTERISTICS

Operating Conditions: VDDA(1,2) = VDDD = 5 V ±5%, GNDA(1,2) = GNDD = 0 V, Tj = -25..90 °C, unless otherwise noted

Item Nr.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
1	VDDA	Permissible Analog Supply Voltage				4.75		5.25	V
2	VDDD	Permissible Digital Supply Voltage				4.75		5.25	V
3	VCMIN	Permissible Offset Voltage for Integration Capacitor				0		1	V
4	I(VDDA)	Supply Current in VDDA					15	20	mA
5	I(VDDD)	Supply Current in VDDD	f(CLK) ≤ 5 MHz				17	20	mA
6	I(VCMIN)	Input Current in VCMIN					10	50	µA
7	Vc()hi	Clamp Voltage hi at AOUT, VCMIN, CLK, DNU, DIN, DOUT	Vc()hi = V(VDDA) - V(); I() = 1 mA, other pins open			0.3		1.5	V
8	Vc()lo	Clamp Voltage lo at AOUT, VCMIN, CLK, DNU, DIN, DOUT	Vc()lo = V(GNDA) - V(); I() = -1 mA, other pins open			-1.5		-0.3	V
Analog Output AOUT									
101	CL()	Permissible Load Capacitance						50	pF
102	Vs()lo	Saturation Voltage lo	I() = 1 mA				300	400	mV
103	Vs()hi	Saturation Voltage hi	Vs()hi = VDDA - V(); I() = -1 mA					400	mV
104	K1	Sensitivity (naked chip)	λ = 880 nm λ = 660 nm λ = 550 nm λ = 470 nm			3.48 6.46 3.69 3.20	4.19 7.78 4.44 3.85	4.74 8.79 5.02 4.35	V/pWs V/pWs V/pWs V/pWs
105	KX	Sensitivity (multi-chip BMST assembly)	λ = 880 nm λ = 660 nm λ = 550 nm λ = 470 nm			3.35 6.22 3.55 3.08	4.19 7.78 4.44 3.85	5.03 9.34 5.33 4.62	V/pWs V/pWs V/pWs V/pWs
106	ΔK1	Sensitivity Nonuniformity	see note (1)			-7.5		7.5	%
107	V0()	Dark Voltage	referenced to VCMIN, integration time is 200 µs				20	100	mV
108	ΔV0()	Dark Voltage Deviation with pixel in track mode	ΔV0() = V0()t1 - V0()t2, Δt = t2 - t1 = 200 µs			-70		70	mV
109	ΔV()	Output Voltage Deviation with pixel in hold mode	ΔV() = V()t1 - V()t2, Δt = t2 - t1 = 200 µs			-2		2	mV
110	ΔV()	Output Voltage Linearity (low level signal)	V() = V0()...0.75 V; see note (2)			-7.5		7.5	mV
111	ΔV()	Output Voltage Linearity (high level signal)	V() = 0.75 V...Vs()hi; see note (3)			-1		1	%
112	V0()rms	Output Voltage Noise (RMS)	V() = 0...4 V, f(CLK) = 5 MHz					2.5	mV
113	VT()	Temperature Voltage	V(CLK) = V(DIN) = 0 V	25		2.9	3.1	3.25	V
114	ΔVT()	Temperature Voltage Coefficient	V(CLK) = V(DIN) = 0 V			-10	-9.5	-9	mV/°C
Photosensor Characteristics									
201	A()	Radiant Sensitive Area	183 µm x 200 µm per pixel				0.037		mm²
202	S(λ)max	Spectral Sensitivity	λ = 680 nm				0.335		A/W
203	λar	Spectral Application Range	S(λar) = 0.25 x S(λ)max			400		950	mm²

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ELECTRICAL and OPTICAL CHARACTERISTICS

Operating Conditions: VDDA(1,2) = VDDD = 5 V ±5%, GNDA(1,2) = GNDD = 0 V, Tj = -25..90 °C, unless otherwise noted

Item Nr.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Digital Inputs DIN, DNU, CLK									
301	Vt()hi	Threshold Voltage hi				1.4	1.5	2.2	V
302	Vt()lo	Threshold Voltage lo				0.8	1	1.3	V
303	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo			300	500	1300	mV
304	Ipd()	Pull-Down Current				10	20	40	µA
305	f(CLK)	Permissible Operating Frequency						5	MHz
306	tw(CLK)lo	Perm. Pulse Width lo at CLK			2	20			ns
307	tw(CLK)hi	Perm. Pulse Width hi at CLK			2	20			ns
308	tw(DIN)hi	Perm. Pulse Width hi at DIN			2	200			ns
Digital Output DOUT									
401	Vs()hi	Saturation Voltage hi	Vs()hi = VDDD - V(), I() = -1 mA				0.1	0.4	V
402	Vs()lo	Saturation Voltage lo	I() = 1 mA				0.1	0.4	V
Low Voltage Detection									
501	VDDDon	Turn-on Threshold VDDD	increasing voltage at VDDD			2.3	2.8	3.8	V
502	VDDDoff	Turn-off Threshold VDDD	decreasing voltage at VDDD			1.2	1.5	1.9	V
503	VDDDhys	Hysteresis	VDDDhys = VDDDon - VDDDoff			0.8	1.3	2	V

Notes : 1) ΔK is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
2) Over the output voltage range given the nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-saturation irradiance levels.
3) As with note #2, here with the maximum deviation given in percent with reference to the ideal analog output voltage.

TIMING CHARACTERISTICS

Operating Conditions: see Electrical and Optical Characteristics, lo = 0...0.45 V, hi = 2.4 V...VDDD.

Item Nr.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I1	tset	Setup time: DIN stable before CLK lo→hi		3	50		ns

Fig. 3: timing definition

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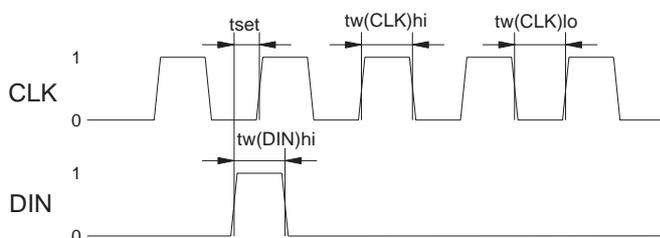
DESCRIPTION OF FUNCTIONS

In the following description it is assumed that DNU is set to lo. If a hi pulse is available at DIN, integration operation of iC-LA is initiated with the next rising edge of the CLK clock signal.

During the first clock cycle all integration capacitors are discharged with the falling edge at CLK. In this clock cycle the chip temperature is output at AOUT. In the second clock cycle all integration capacitors are precharged to VCMIN; with the falling edge of the clock signal all 64 pixels start to be integrated.

In this clock cycle all track-and-hold circuits are in hold mode; the voltage of the pixel 0 track-and-hold capacitor is switched to AOUT. This voltage is initially unknown as the track-and-hold capacitors of a pixel have not been reset. With the rising edge of the third clock cycle pixel 0 changes into track mode. With this, the voltage of the pixel 1 track-and-hold capacitor is switched to AOUT, which again is unknown. With the rising edge of the next clock cycle pixel 1 changes into track mode and the voltage of the track-and hold-capacitor from pixel 2 is switched to AOUT.

At the 66th clock cycle the temperature is available at AOUT, completing the initialization of the device (initial run). The stored integration voltages from the initial run are available at AOUT during the next run.

If a new hi pulse is available at DIN, a complete new integration cycle starts (run 1) and the sequence of the device repeats. In the first clock cycle of run 1 all track-and-hold circuits again switch into hold mode; all integration capacitors are discharged. During the second clock cycle all integration capacitors are recharged to VCMIN and the integration process restarts.
Between this and the 66th clock cycle the pixel voltages stored in the previous integration cycle in the track-and-hold capacitors are present at AOUT for the duration of one cycle.

It again takes 66 clock cycles for the voltages from all of the switch-and-hold capacitors to be read out. The last clock cycle again outputs the chip temperature and completes the run. Continuous operation of the device is obtained when DIN is again given a hi signal after a run has been completed by the 66th clock cycle.
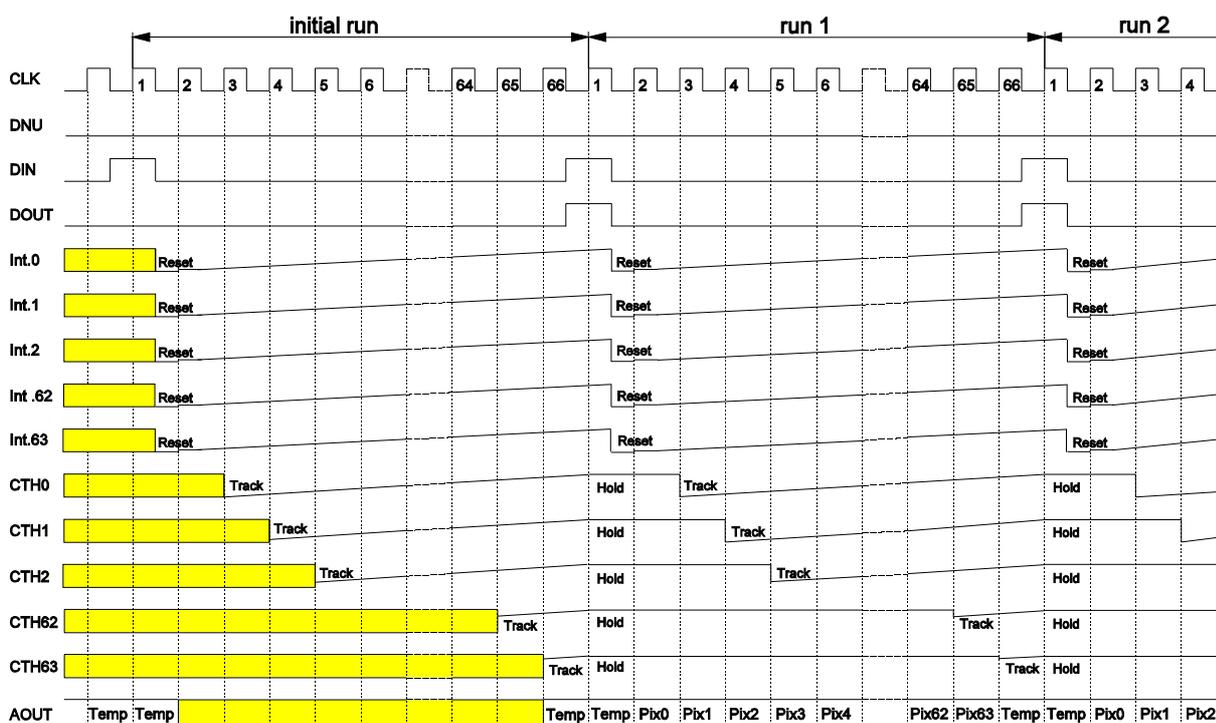

Fig. 4: timing diagram

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ORDERING INFORMATION

Type	Package	Order designation
iC-LA	-	iC-LA chip

For information about prices, terms of delivery, options for other case types, etc., please contact:

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