iC-MCW

BiSS WATCHDOG FOR RS422 WITH SPI

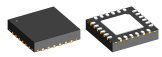
FEATURES

- Acquisition of BiSS Single Cycle Data
- Acquisition of BiSS Control Data
- Monitoring of BiSS Communication Status
- Analysis Data of BiSS Protocol
- Error Diagnostics for Debugging
- Pin for Simple Error Indication
- Automatic Compensation of Line Delay and Processing Times
- Internal 14-bit BiSS Frame Counter
- Built-In RS422 Receiver for Direct Interfacing with BiSS
- Support of BiSS Data Transfer Rates of up to 10 MBit/s
- Serial Controller Communication via SPI™ Slave Interface
- Support of Interrupt-Driven I/O
- Built-In System and High Speed Sample Clock Generation
- Built-In Power on Reset
- 3.3 V to 5 V Supply (+/-10%)
- Industrial Temperature Range

APPLICATIONS

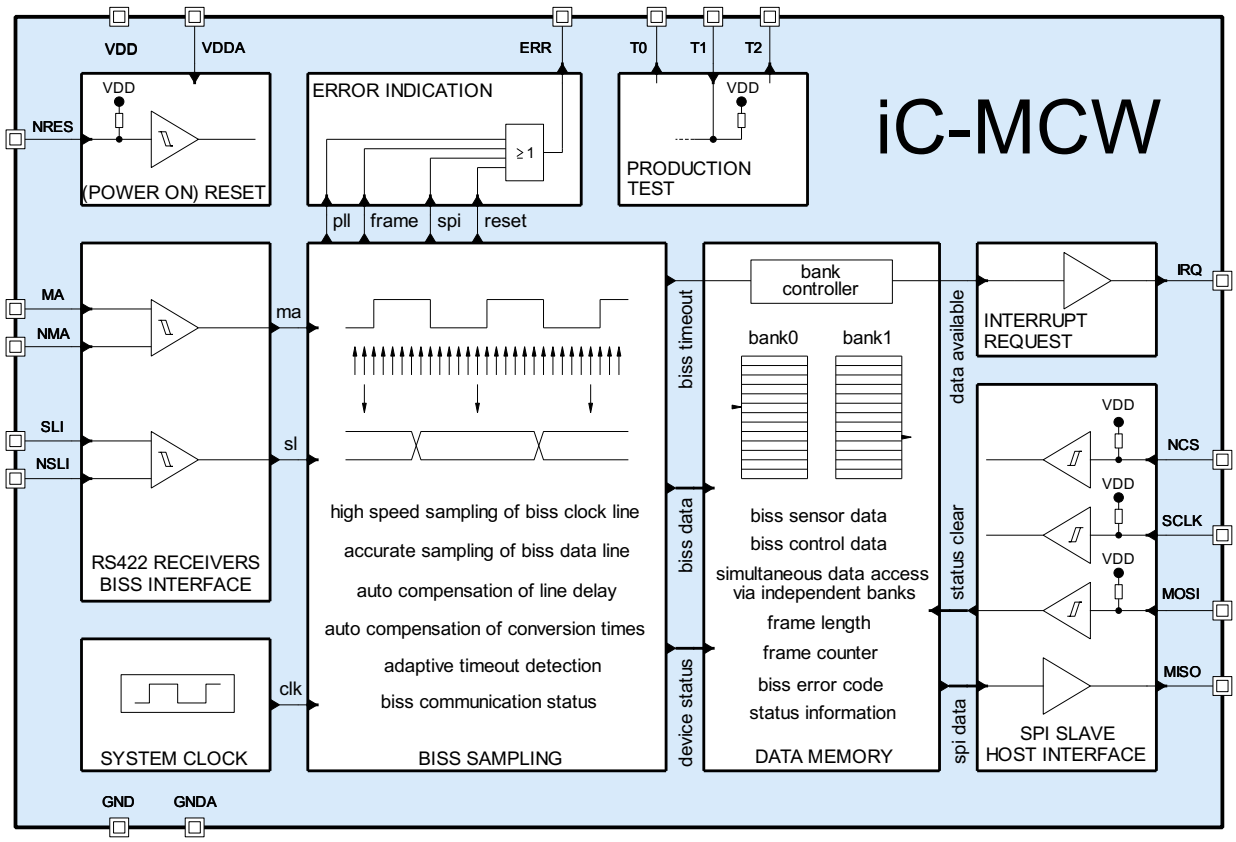
- BiSS Communication Monitoring
- BiSS Safety Extension of BiSS Standard Drives
- BiSS Safety Drives

PACKAGES



QFN24-4x4

BLOCK DIAGRAM



DESCRIPTION

The iC-MCW is a BiSS C communication monitoring device to be connected to a microcontroller via standard SPI. The integrated circuit observes the BiSS C protocol sequence and samples sensor and control data at maximum transmission rates of 10 MBit/s. The iC-MCW includes RS422 receivers to be connected to the differential BiSS transmission lines directly. Due to built-in clock generation, the chip does not need any external oscillators.

An adaptive BiSS timeout detects the end of a received BiSS frame and triggers an interrupt request to notify the microcontroller about new BiSS communication status and frame data. Alternatively, it is possible to constantly poll the chip status, which indicates the availability of new frame data as well.

The frame data is stored in internal random access memory, which is organized into two banks. Hence, current frame data can be read through the SPI interface while a new BiSS frame is sampled. If the frame data of one bank has not been fetched in time, it will be overwritten with new frame data. iC-MCW informs the microcontroller about lost frames indirectly by counting the BiSS timeout of each incoming BiSS frame. The internal frame counter is available through SPI as well.

Detailed status and error information are available by register access. Critical errors are mapped to the error pin and must manually be reset via SPI.

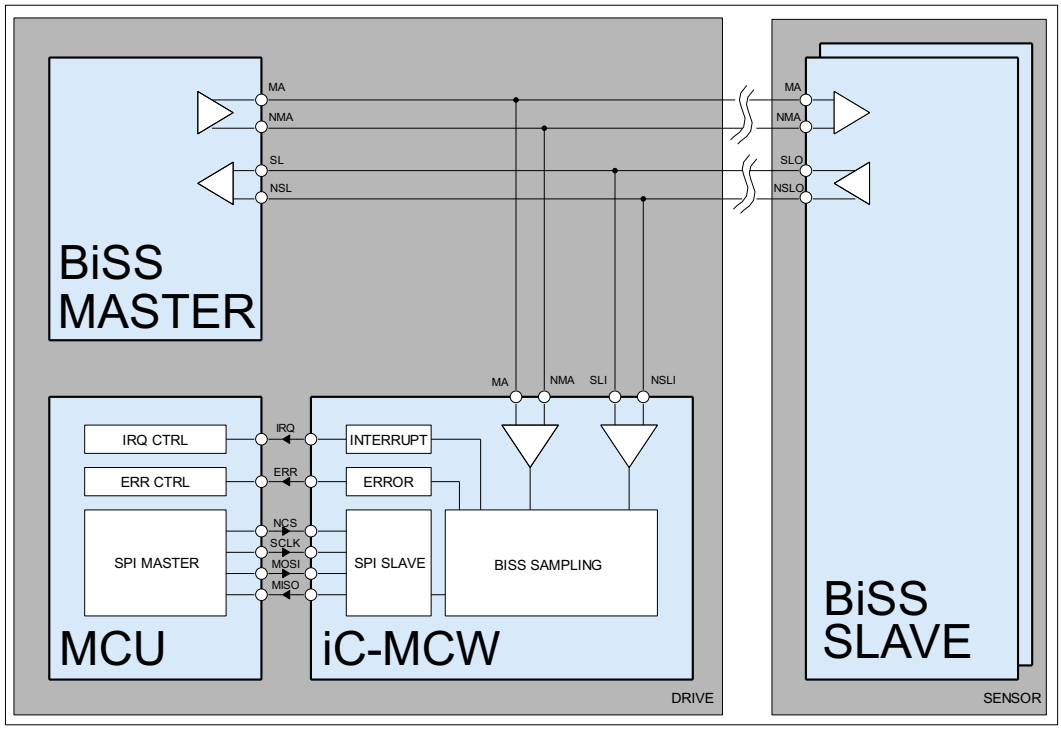
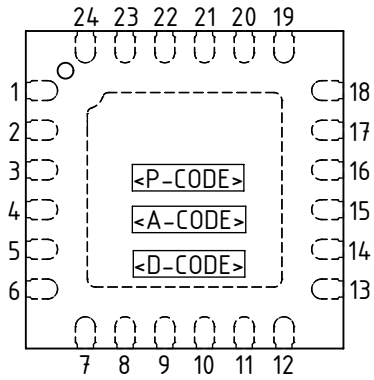


Figure 1: Integration of the iC-MCW in a BiSS Communication System

Figure 1 shows the extension of a BiSS communication system with iC-MCW. The standard drive establishes a common differential BiSS communication line to one or more BiSS slaves by BiSS master. The BiSS clock and BiSS data lines are connected to the RS422 receiver within the iC-MCW. The microcontroller is connected to the SPI interface of iC-MCW and can import the BiSS frame data without disrupting the transmission between BiSS master and BiSS slave. Thus, it is possible to implement any additional features to extend the standard drive to match safety requirements, for example.

PACKAGING INFORMATION TO JEDEC

PIN CONFIGURATION QFN24 4mm x 4mm



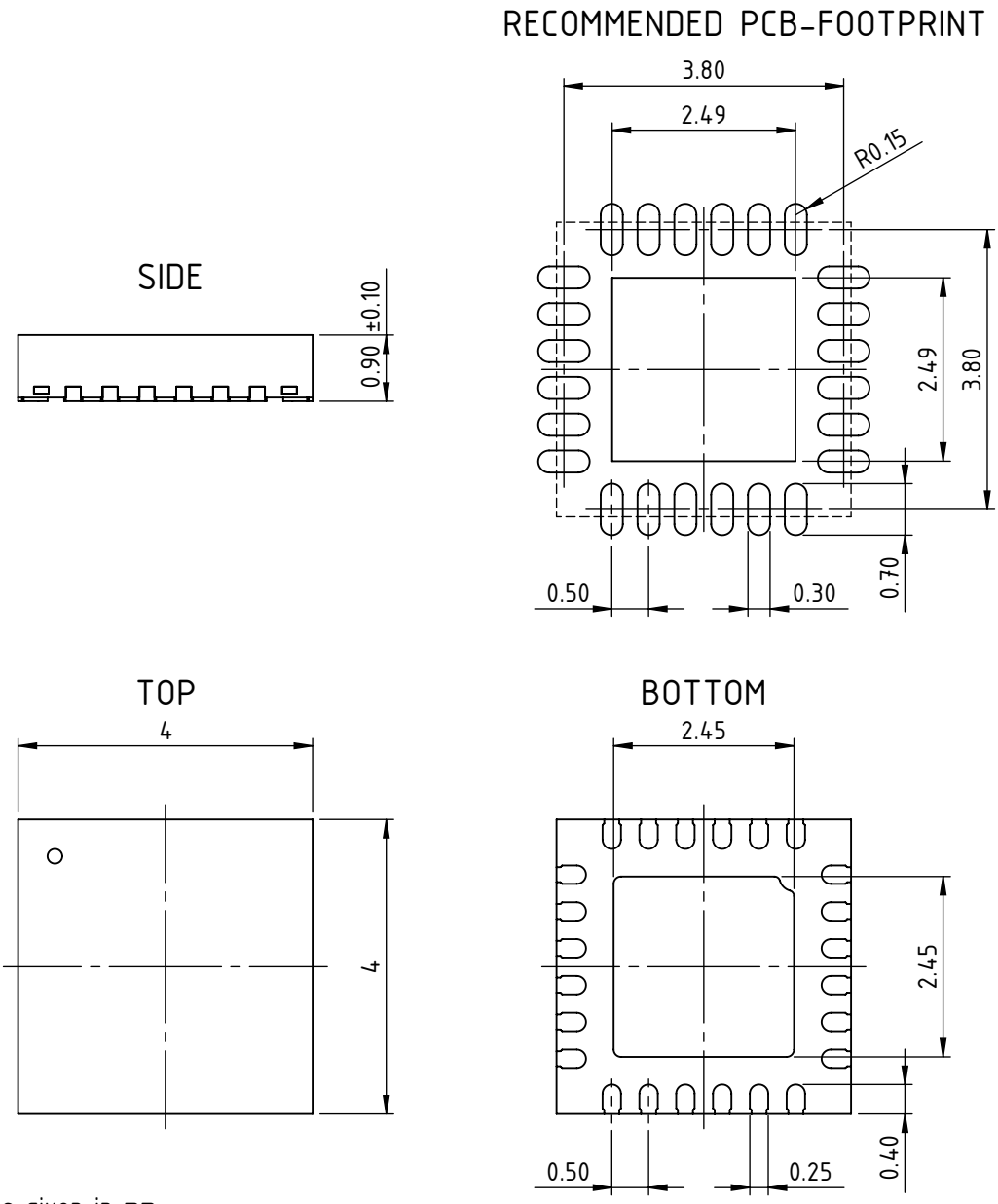
PIN FUNCTIONS

No.	Name	Function
1	T0	Test Pin [1]
2	n.c.	[2]
3	VDDA	+3.3 V . . . +5 V Analog Supply Voltage
4	n.c.	[2]
5	GNDA	Analog Ground
6	n.c.	[2]
7	n.c.	[2]
8	n.c.	[2]
9	SLI	BiSS Data Line Input
10	NSLI	BiSS Data Line Input (inverted)
11	MA	BiSS Clock Line Input
12	NMA	BiSS Clock Line Input (inverted)
13	n.c.	[2]
14	IRQ	Interrupt Request Output
15	GND	Digital Ground
16	T1	Test Pin [3]
17	NRES	Reset Signal Input (low active)
18	ERR	Error Output
19	MOSI	SPI Serial Data Input
20	MISO	SPI Serial Data Output
21	NCS	SPI Chip Select Input
22	SCLK	SPI Clock Input
23	VDD	+3.3 V . . . +5 V Digital Supply Voltage
24	T2	Test Pin [1]
	BP	Backside Paddle [4]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes).
1) Test Pins T0 and T2 shall not be connected.
2) Pin numbers marked n.c. are not connected.
3) Test Pin T1 is low active, requires external high for normal operation.
4) Connecting the backside paddle to GNDA is recommended. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS QFN24 4mm x 4mm

All dimensions given in mm.



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Supply Voltage VDD		-0.3	6	V
G002	I(VDD)	Current in VDD		-100	150	mA
G003	VDDA	Analog Supply Voltage VDDA		-0.3	6	V
G004	I(VDDA)	Current in VDDA		-100	150	mA
G005	V()	Voltage at all pins, excluding VDD, VDDA, GND and GNDA		-0.3	6	V
G006	I()	Current in all pins excluding VDD, VDDA, GND and GNDA		-100	150	mA
G007	V_{esd}()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G008	Tj	Operating Junction Temperature Range		-40	125	°C

THERMAL DATA

Operating Conditions: VDD = 3.0 V ... 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		115	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN24-4x4 package mounted on PCB, thermal pad at approx. 6 cm² cooling area		80		K/W
T03	Ts	Storage Temperature	QFN-4x4	-40		85	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = VDDA = 3.0 V ... 5.5 V, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD, VDDA	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current in VDD	VDD=3 V, outputs not loaded VDD=5.5 V, outputs not loaded	2 4	5 10	8 16	mA mA
003	I(VDDA)	Supply Current in VDDA	VDDA=3 V, outputs not loaded VDDA=5.5 V, outputs not loaded	130 160	330 400	530 640	µA µA
004	Vc()hi	Clamp Voltage hi at all pins excluding VDD, VDDA, GND, GNDA	Vc()hi = V() - VDD, I() = 1 mA	0.3		1.5	V
005	Vc()lo	Clamp Voltage lo at all pins excluding VDD, VDDA, GND, GNDA	Vc()lo = V(), I() = -1 mA	-1.5		-0.3	V
SPI Host Interface: NCS, SCLK, MISO, MOSI							
A01	Vs()hi	Saturation Voltage hi at MISO	Vs()hi = VDD - V() I() = -1.6 mA			400	mV
A02	Vs()lo	Saturation Voltage lo at MISO	Vs()lo = V() I() = 1.6 mA			400	mV
A05	Vt()hi	Threshold Voltage hi at NRES, NCS, SCLK and MOSI				70	%VDD
A06	Vt()lo	Threshold Voltage lo at NRES, NCS, SCLK and MOSI		30			%VDD
A07	Vt()hys	Threshold Voltage Hysteresis at NRES, NCS, SCLK and MOSI		200			mV
A08	Ipu()	Pull-Up Current at NRES, NCS, SCLK and MOSI	V() = 0 V..VDD - 1 V VDD = 3 V VDD = 5.5 V	 -16 -61		 -3.3 -7	 µA µA
A09	fclk()	Permissible Clock Frequency at SCLK		10			MHz
A10	T_{int}	Interrupt Time		4.5	5.6	8	µs
RS422 BiSS Interface: MA, NMA, SLI, NSLI							
B01	Vin()	Permissible Input Voltage		-10		10	V
B02	Vcm()	Input Common Mode Voltage		-7		7	V
B03	Vdiff()	Differential Input Voltage	Vdiff() = V(MA) - V(NMA)	-12		12	V
B04	Rin()	Input Resistance	MA/SLI vs GND, NMA/NSLI vs GND	4			kΩ
B05	Vt()hi	Differential Input Threshold hi	Vdiff(MA/SLI) = V(MA/SLI) - V(NMA/NSLI)			200	mV
B06	Vt()lo	Differential Input Threshold lo	Vdiff(MA/SLI) = V(MA/SLI) - V(NMA/NSLI)	-200			mV
B07	Vt()hys	Differential Input Hysteresis	Vdiff(MA/SLI) = V(MA/SLI) - V(NMA/NSLI)	5	55		mV
B08	fclk()	Permissible Frequency at MA		10			MHz
B09	tout()	Adaptive BiSS Timeout			1.5 x 1/fclk		
B10	T_{Smp}	Internal Sample Period		4.8		9	ns
Ports: IRQ, ERR, NRES							
C01	Vs()hi	Saturation Voltage hi at IRQ and ERR	Vs()hi = VDD - V() I() = -1.6 mA			400	mV
C02	Vs()lo	Saturation Voltage lo at IRQ and ERR	Vs()lo = V() I() = 1.6 mA			400	mV
C05	Vt()hi	Threshold Voltage hi at NRES				70	%VDD
C06	Vt()lo	Threshold Voltage lo at NRES		30			%VDD
C07	Vt()hys	Threshold Voltage Hysteresis at NRES		200			mV
C08	Ipu()	Pull-Up Current at NRES	V() = 0 V..VDD - 1 V VDD = 3 V VDD = 5.5 V	 -16 -61		 -3.3 -7	 µA µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = VDDA = 3.0 V ... 5.5 V, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Internal Oscillator:							
D01	fosc	Internal Oscillator Frequency		16	23	30	MHz
Power-On Reset:							
E01	VDDon	VDDA Turn-On Threshold	VDDA increasing	2.79		2.96	V
E02	VDDoff	VDDA Turn-Off Threshold (Undervoltage Reset)	VDDA decreasing	2.61		2.78	V
E03	VDDhys	Undervoltage Hysteresis	VDDhys = VDDon - VDDoff	40	180		mV

OPERATING REQUIREMENTS: BiSS Interface - BiSS C Frame

Operating conditions: VDD = VDDA = 3.0 ... 5.5 V, Tj = -40 ... 125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Sensor Data Cycle						
I001	T_{MAS}	Clock Period		80	12500	kHz
I002	t_{pLine}	Permissible Line Delay			unlimited	
I003	Δt_{pL}	Permissible Propagation Delay Jitter	Δ tpL = max(|tpLine - tpLx|); x= 1 ... n		12.5	% T_{MAS}
I004	T_{tos1}	Adaptive BiSS Timeout		1.5xT_{MAS} - 2xT_{Smp}	1.5xT_{MAS} + 2xT_{Smp}	
I005	T_{tos2}	Static BiSS Timeout		12.5	40	µs

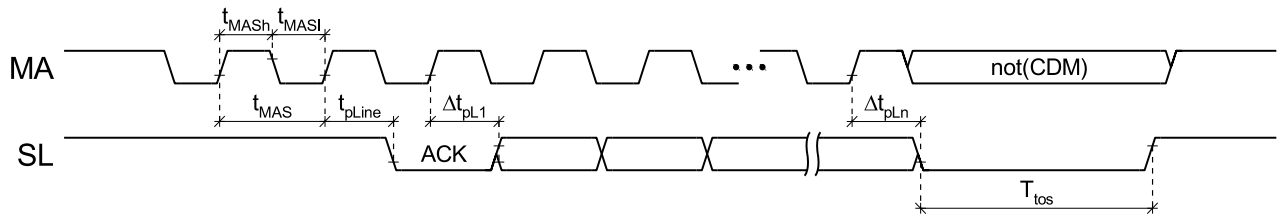

Figure 2: Timing Diagram BiSS Frame

OPERATING REQUIREMENTS: Host Interface, SPI mode

Operating Conditions: VDD = VDDA = 3.0 ... 5.5 V, Tj = -40 ... 125 °C;
Lo Input Level = 0 V, Hi Input Level = VDD, Lo Output Level = 0 V, Hi Output Level = VDD
Capacitive Load at MISO = 20pF

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{C1}	Permissible Cycle Time		100		ns
I102	t_{W1}	Wait Time: NCS lo → hi to NCS hi → lo		100		ns
I103	t_{S1}	Setup Time: NCS lo before SCLK lo → hi		50		ns
I104	t_{P1}	Propagation Delay: MISO stable after NCS hi → lo			50	ns
I105	t_{P2}	Propagation Delay: MISO hiZ after NCS lo→ hi			50	ns
I106	t_{H1}	Hold Time: NCS lo after SCLK lo → hi		50		ns
I107	t_{S2}	Setup Time: MOSI stable before SCLK lo → hi		10		ns
I108	t_{H2}	Hold Time: MOSI stable after SCLK lo → hi		10		ns
I109	t_{P4}	Propagation Delay: MISO stable after SCLK hi → lo			47	ns

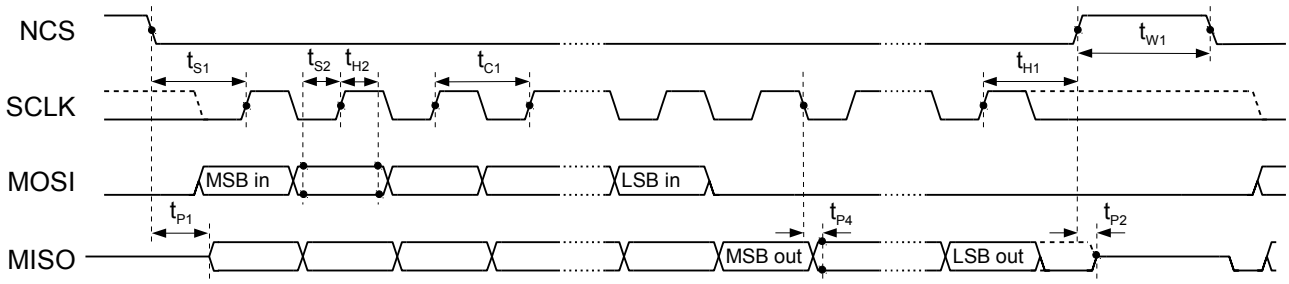

Figure 3: SPI Access

REGISTER LAYOUT

The register bank of the iC-MCW can be accessed via SPI command Read Register and Write Register. Table 7 gives an overview of the available chip addresses and data.
It is possible to read multiple register addresses successively by continuing to generate SPI clocks after the data of the first address has been clocked out.
Invalid read or write addresses trigger an error to the register DeviceError and pin ERR.

Chip Revision

iC-MCW's chip revision CHIP_REV can be read via SPI to test the status of iC-MCW and the SPI communication system.

CHIP_REV	Addr. 0x00; bit 7:0	R
Code	Chip Revision	
0xB2	MCW_Z1	
0xC1	MCW_Y	
Other	Reserved	

Table 6: Chip Revision Values

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ChipRevision (R)								
0x00	CHIP_REV[7:0]							
DeviceStatus (R)								
0x01	RESERVED			AVAIL	DETECT	STATE[2:0]		
DeviceError (R/W)								
0x02	SFRAME	PLL	RESERVED	OPCODE	READ	WRITE	HFRAME	RST
FrameInformation (R)								
0x03	INFO[7:0]							
FrameNumberCD (R)								
0x04	FNUM[7:0]							
0x05	CDS	NCDM	FNUM[13:8]					
FrameError (R)								
0x06	RESERVED					CODE[2:1]		WARN
RESERVED: 0x07..0x0B								
0x07 ... 0x0B	RESERVED (Do not write)							
BiSS Measurement (R)								
0x0C	C_TIME[7:0]							
0x0D	L_DELAY[2:0]			C_TIME[12:8]				
0x0E	P_TIME[0]	L_DELAY[9:3]						
0x0F	P_TIME[8:1]							

Table 7: Register layout

The error bits in register DeviceError are persistent and must be reset manually by sending the SPI command Write Register to this register.

ELECTRICAL CONNECTIONS

Power Supply

To put the iC-MCW into operation, all that is needed is a power supply of 3.3 V up to 5 V. Two 100 nF external buffer capacitors between VDD/VDDA and GND/GNDA and one 1 nF external buffer capacitor between VDD and GND stabilize the input voltages of the iC-MCW. Since the analog and digital power supplies are separate, VDD and VDDA as well as GND and GNDA must be at the same voltage level. Furthermore, GND and GNDA must be connected as short as possible. Figure 4 illustrates the connection of the iC-MCW for a typical use case.

System Clock

Due to its internal Phase Locked Loop (PLL) driven oscillator, the iC-MCW does not need any external clock source. The high precision sample clock is generated independently. In case of problems with the sample clock generation, an error is reported to the chip status.

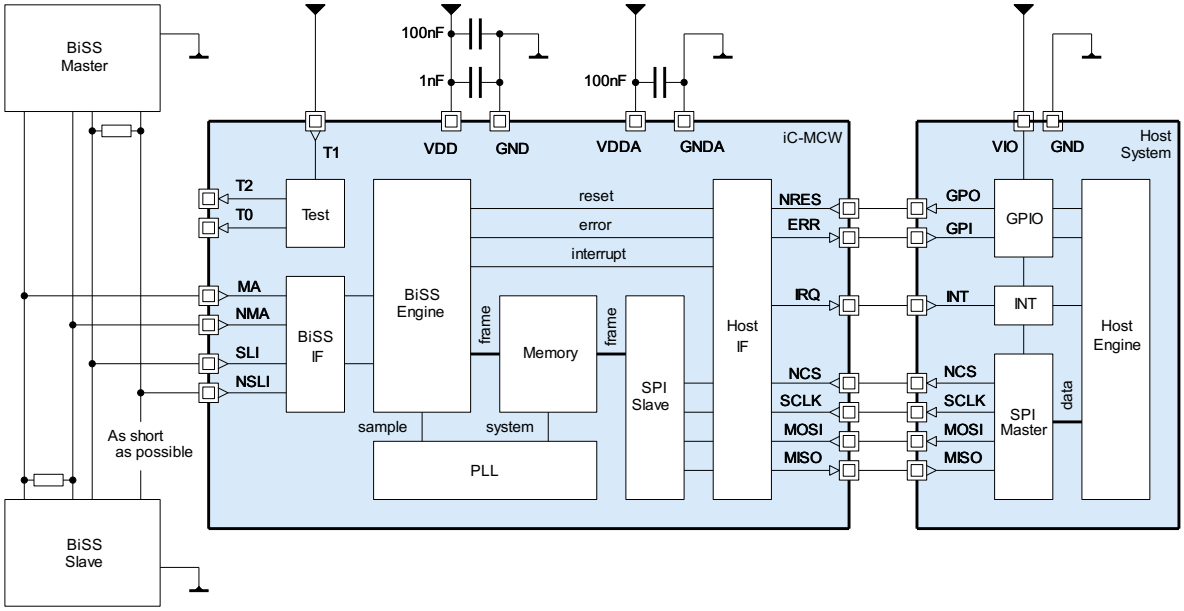

Figure 4: Connections of the iC-MCW

Digital Input

All digital input pins have internal pull-up circuits to provide a default chip state when floating. It is recommended to support unused digital input pins by directly connecting the external power supply voltage. Table 8 shows the essential digital input pins of iC-MCW.

Name	Pin	Function
T1	16	Test Enable
NRES	17	Chip Reset
NCS	21	SPI Chip Select

Table 8: Essential Input Pins

BiSS Interface

Since RS422 receivers are included in iC-MCW's BiSS interface, the differential BiSS clock line and data line can be connected to the corresponding pins MA/NMA and SLI/NSLI directly.
The iC-MCW is a pure BiSS listener and can only be used to extend a complete BiSS communication system. The BiSS communication system consists of one BiSS master and one or more BiSS slaves connected via RS422 standard. As shown in Figure 4, the RS422 standard suggests suitable termination resistors to allow high frequency data transmission. The additional connection to iC-MCW does not need any external resistors for signal termination. However, the connection between the BiSS transmission line and iC-MCW must be designed to be as short as possible to avoid signal reflections.
The BiSS interface follows the electrical specification of the RS422 standard.

Host Interface

A common 4-wire Serial Peripheral Interface (SPI) offers communications between the iC-MCW and a host system, e.g. a microcontroller. The iC-MCW supports SPI transmissions with data rates of up to 10 MHz, if common high frequency connection concepts are being considered.

For use in interrupt-driven I/O systems, an interrupt request pin IRQ is available. Whenever new BiSS frame data is available, the IRQ produces an interrupt impulse, that can be observed by the host system.
The error pin ERR can be connected to a general input line of the host system to quickly evaluate the error status of the iC-MCW without triggering an additional SPI transfer.

A simple general purpose output connection to the external reset pin NRES allows the host system to reset the iC-MCW to its defined start state whenever necessary.
The digital I/O voltage levels of the host interface are defined by VDD and GND. Except for the BiSS Interface, the whole system must be connected to the same power supply voltage.

START-UP

Power On Reset

After connecting a power supply to iC-MCW, the internal Power On Reset (POR) puts the chip into its defined start state. The reset signal is removed as soon as the required power supply voltage is reached and the PLL delivers a stable system clock.

The analog power supply must not be ramped up before the digital power supply.

After system restart or an external reset signal at pin NRES, error bit RST of the chip status is set. Since the error bits must be reset manually via SPI, an unintentional chip reset will always be detected. More information about the chip status can be found in chapter MODE OF OPERATION.

BiSS Frame Counter

The BiSS frame counter (FCNT) is an important safety feature of the iC-MCW. The sign-of-life counter within the BiSS protocol ensures data consistency at the host system. If the process cycle time of the host system does not match the frame cycle time of the BiSS system, the internal frame counter can be used to count lost BiSS frames. The frame counter's value is accessible through parameter FNUM.
At start-up or after an external reset signal at NRES, the frame counter is reset to zero.

BiSS Measurement: Cycle Time

The optional BiSS Measurement C_TIME represents the time in between two consecutive BiSS frames. After start-up, the first C_TIME is measured from POR to the first rising edge on MA of the first BiSS frame.

Chip Configuration

iC-MCW is a robust device with a single data path. For safety reasons, there is no internal chip configuration to alter the behavior of iC-MCW. Any setup concerning the BiSS protocol is exclusively done within the host system.

MODE OF OPERATION

Once activated, the iC-MCW constantly observes the BiSS communication lines. The transitions of iC-MCW's internal logical states are triggered by specific events on MA or SLI.

System States

There are eight logical states the iC-MCW cycles through during BiSS frame processing. Each state handles the signaling of a specific stage of the BiSS communication. STATE is the corresponding code for the currently active state that can be read via SPI command Read Register.
The logical states can be mapped to the different frame sections of a BiSS C frame as shown in Figure 5. The system states are shown in red on top of the MA clock signal.

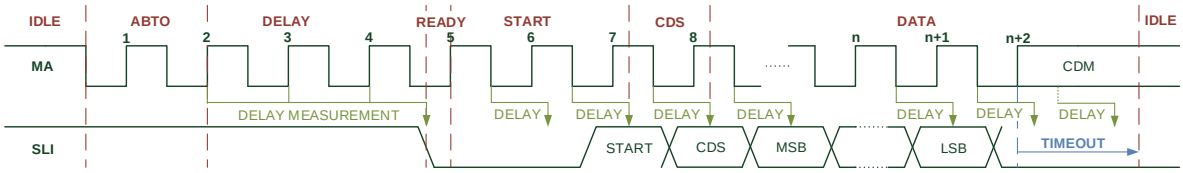

Figure 5: BiSS Frame

STATE	Addr. 0x01; bit 2:0	R
Code	System State	Task
0b000	IDLE	Waiting for Frame Start
0b001	ABTO	Measurement of the Adaptive BiSS Timeout
0b010	DELAY	Measurement of the BiSS Line Delay
0b011	READY	Waiting for Clock Cycle
0b100	START	Waiting for Start Bit
0b101	CDS	Sampling of CDS Bit
0b110	DATA	Sampling of Sensor Data
0b111	ERROR	Waiting for BiSS Timeout

Table 9: System States of iC-MCW

State IDLE:
Waiting for Frame Start
As long as the connected BiSS clock line MA is digital high, iC-MCW stays in state IDLE waiting for a new BiSS communication to start. The BiSS cycle time in between the beginning of two consecutive BiSS frames is measured and can be read by the SPI. A timer in the host system can be used to check idle times between two BiSS frames that exceed the internal timer of iC-MCW.
A new BiSS communication starts with a falling edge on BiSS clock line MA. As shown in Figure 5 SLI is supposed to be digital high at this point. If SLI is digital low at the start of the communication, the BiSS frame will be reported as erroneous by a flagged error bit in the DeviceError register and at the external error pin ERR. However, the BiSS frame is still processed until the BiSS timeout is detected.

State ABTO:
Measurement of the Adaptive BiSS Timeout
While the adaptive BiSS timeout (ABTO) is measured, the static BiSS timeout (SBTO) is used to determine the end of a BiSS frame. iC-MCW observes the BiSS clock line MA and starts the SBTO counter as soon as a new BiSS communication begins. The timeout counter is reset for every change of the voltage level at MA. If an SBTO is detected, iC-MCW sets an error bit in the chip status, generates an interrupt request at pin IRQ and goes back to state IDLE.
The ABTO is measured during the first 1.5 MA clock periods. If the second rising edge at MA has been detected, the iC-MCW recognizes a BiSS timeout whenever there are no further changes within that measured period of time. It can be important to extend the first 1.5 MA clock periods, if an SPI master interface is used to emulate the BiSS C protocol for example. The maximum time for the ABTO is the SBTO.

State DELAY:
Measurement of the BiSS Line Delay
iC-MCW is capable of compensating line delays between the rising edge of MA triggered by the BiSS master and the corresponding response of the BiSS slave on the data line SLI. The line delay measurement starts at the second rising edge of MA and can be read via SPI to analyze the BiSS communication. If SLI is already digital low at the beginning of the line delay measurement, iC-MCW continues to the logical state ERROR and sets an error bit in register DeviceStatus to report an invalid BiSS protocol.
While there is a maximum value of the delay timer, the delay compensation is not limited, since it works on a cycle by cycle basis.

If there is no response by the BiSS slave, only the BiSS master is responsible to stop generating MA clock cycles.

Figure 5 shows the line delay measurement in between MA and SLI colored in green. Once measured, the line delay is used for determining the optimum sample point of data bits received on the line SLI.

State READY:
Waiting for next Clock Cycle
After measuring the line delay, iC-MCW waits for the next clock cycle of the BiSS frame to begin. At this point, the optimum sample point of the BiSS data line can be used to sample the frame data. The logical state is READY.

State START:
Waiting for Start Bit and BiSS Processing Time
Before any data is transmitted, the BiSS slave sends the start bit to inform the BiSS master that the requested data is available. The start bit can be delayed by the slave if additional processing time is needed to provide the data. The iC-MCW measures the processing

time within the state START until the start bit is recognized. The processing time P_TIME can be read via SPI. While the timer of the processing time is limited, iC-MCW remains in the state START until the start bit is recognized or the frame is canceled by an ABTO.

The processing time has to be managed by the BiSS master.

State CDS:
Sampling of CDS Bit (BiSS Control Data)
BiSS Control Data bits are sampled by iC-MCW in both directions. The CDS bit is sampled after the start bit has been detected successfully. The NCDM bit on the other hand is read at the end of a BiSS frame when the timeout occurs. The BiSS Control Data is not concatenated by the iC-MCW and must be loaded for each BiSS frame separately. CDS and NCDM bits of the last BiSS frame can be read via SPI.
More information about the BiSS Control Data can be found in chapter HOST INTERFACE on page 16.

State DATA:
Sampling of Sensor Data
Since iC-MCW does not need to be configured to any specific BiSS frame data length, the chip will accept BiSS frames of any data lengths until the memory limit is reached. That means BiSS frames with a data length of 0...250 bits will be accepted without any error triggered.
In general iC-MCW supports three classes of BiSS frames that are shown in Table 10.
iC-MCW samples all bits of the BiSS frame until an ABTO is recognized. It is possible, that the iC-MCW samples more bits than generated by the BiSS slave. That is because the BiSS master toggles the MA line until the number of configured data bits is processed. The additionally sampled bits do not carry any information and must be omitted by the host system. The number of sampled bits is stored internally and is accessible via SPI.

The frame data is written to the internal random access memory (RAM). Since each RAM cell contains one byte of data, the BiSS frame is divided into 8 bit chunks. The BiSS frame, which is sent MSB-first, is shifted into the LSB of each memory cell. Figure 6 illustrates an example frame of 29 bits written into the memory.

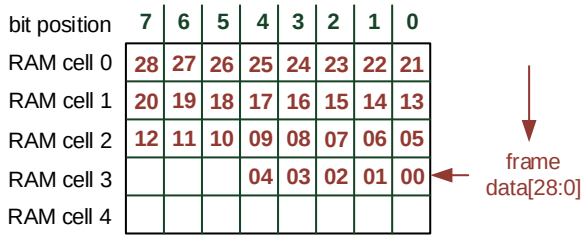

Figure 6: Example Frame in RAM

The last byte of each frame may be incompletely filled. The host system must be configured to the expected frame length to correctly mask the last byte. More information about masking the last byte can be found in section HOST INTERFACE on page 16.

BiSS Frame	Description
Reduced Frame	The reduced frame can be used to send broadcast commands to unconfigured BiSS slaves. The frame is completed when the adaptive BiSS timeout is detected in the logical state DELAY or READY.
Short Frame	A short frame is a BiSS frame with a data length of zero. Only CDS and NCDM bits are exchanged between master and slave. It is used for fast register communication during configuration.
Standard Frame	A standard frame is a BiSS frame that is configured to transmit sensor data of a specific length within each frame cycle. Simultaneously, the CDS and NCDM bits are transmitted to provide control data communications. This is the standard BiSS operation.

Table 10: Classes of BiSS Frames

State ERROR:
Waiting for BiSS Timeout
As described in section State ABTO the Control Data bit NCDM is read at the end of the BiSS Frame when the timeout occurs. Depending on the logical state the iC-MCW is operating in, a BiSS timeout might trigger an error. According to the BiSS C protocol, a BiSS timeout occurring in the logical states ABTO, START and CDS is not allowed. An error will be reported to the DeviceStatus and the error pin ERR.

Host System
There are two ways to inform the host system about new BiSS frame data. First, the iC-MCW generates an

interrupt request every time a BiSS timeout occurs and the memory bank can be switched to make the frame data accessible. The interrupt pin IRQ is held digital high for a specific time or until an SPI transfer has been started by the host system. The duration of the IRQ pulse restricts the minimum BiSS frame period of the communication system.
Second, it is possible to poll the chip status and observe the bit DETECT that is set every time a BiSS timeout occurs. Since the Frame Counter (FCNT) is also incremented every time a BiSS timeout occurs, the bit DETECT is digital high if FCNT is not zero. However, the bit DETECT only reports a complete BiSS frame detected by iC-MCW. Due to memory bank access collisions, the frame data is only available if the bit AVAIL is set as well. Thus, AVAIL matches the activation of an interrupt request.
Figure 7 shows the status bits above during execution of a chip communication sequence that is described in detail in the following section. The FCNT as well as AVAIL and DETECT are reset every time the frame data of the iC-MCW is accessed via SPI.
FNUM contains the value of FCNT that is temporarily frozen to be accessible via SPI.

The maximum value of FNUM is 0x3FFF. If further BiSS frames are lost, FNUM retains its maximum value and does not restart from zero until frame data is accessed via SPI.

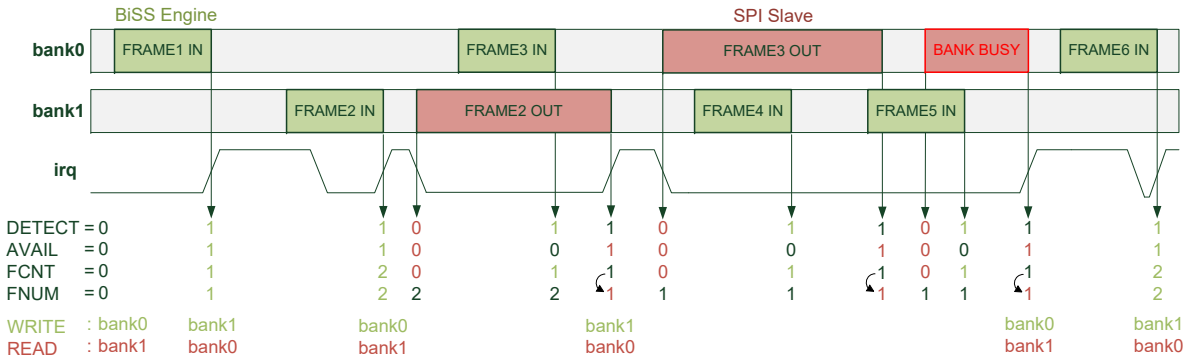

Figure 7: Memory Bank Access

Memory Banks
The frame data memory of the iC-MCW is organized into two independent banks. Each frame bank can hold 250 frame bits which correspond to three fully configured BiSS frames with 16-bit CRC protection for each channel.
Figure 7 shows the bank selection, the interrupt request generation and the corresponding status bits during an example frame write and read sequence. The incoming BiSS frames, that are written into the memory of iC-MCW are colored in green, the reading by the host via SPI is colored in red.
If there is no SPI transmission in progress, new frame data is written to the memory banks alternately. The bank selection for read access is accordingly set to the memory bank that holds the newest frame data. The FCNT is incremented whenever a new frame transmission is completed by the BiSS timeout. The bits DETECT and AVAIL report new frame data that can be read via SPI. The interrupt request is directly set and can be used to implement interrupt-driven I/O applications.
During a frame data transmission via SPI, incoming BiSS frame data is written into the second memory bank simultaneously. If the SPI command is not completed at the end of the incoming BiSS frame, DETECT is set and the FCNT is incremented but AVAIL and the interrupt request at pin IRQ is delayed until the end of the SPI frame.
Since switching of the memory banks is also delayed, another incoming BiSS frame overwrites the data of the previous BiSS frame as long as iC-MCW is busy accessing frame data via SPI. Thus, iC-MCW allows the access of one BiSS frame (FRAME3 OUT) until the second incoming BiSS frame (FRAME5 IN) begins.
However, lost BiSS frames are captured by FCNT that is transmitted as FNUM during SPI command Read Frame Data supporting the safety related sign-of-life counter even for slower host systems.
If the read and write access overlap, there is no interrupt request generated and the INFO Byte reports BANK_BUSY to mark the received data as invalid.
More information about the SPI opcodes can be found in section HOST INTERFACE on page 16.

BiSS Frame Data
The iC-MCW is a BiSS to SPI bridge only and does not analyze any BiSS frame data. The extraction of the sensor data and data consistency checks, like CRC calculation, is intended to be done by the host system. Hence, the host system must exactly be configured just as the connected BiSS slave to interpret the BiSS frame data of the iC-MCW correctly.

HOST INTERFACE

The host interface of the iC-MCW consists of pins NRES, IRQ, ERR and the 4 SPI pins. It is suitable for applications that use interrupt-driven I/O or chip status polling.

Pin NRES

The pin NRES is intended to set the iC-MCW back to its defined start state. It provides the functionality to test if the BiSS lines are properly connected to the iC-MCW. However, because of the internal POR the external NRES pin can be left unconnected.

Pin IRQ

An interrupt request IRQ is generated every time a new BiSS timeout is detected and the memory bank is ready to switch the address selection for read access. It does not matter what kind of BiSS frame is transmitted or if there are any errors during communications, the IRQ pin indicates new data is available.
After a BiSS timeout, the interrupt request at pin IRQ is digital high for a specific time T_{int} only (see Elec. Char. A10). Every SPI transmission acknowledges the current interrupt request by resetting the interrupt pin even before the specific time runs out.
The pin IRQ is intended to be used in systems that support interrupt-driven I/O.

Pin ERR

The pin ERR is generated by a logical OR gate connected to all error bits of the register DeviceError. For interrupt-driven I/O systems, the pin ERR can be used to observe the register DeviceError without sending any SPI opcode. Only if pin ERR is set, an SPI command is needed to get detailed information about the error occurred.
The error bits and the error pin can only be reset by sending the SPI command Write Register to the register DeviceError.

SPI Mode

iC-MCW provides an SPI slave to communicate with the host system. The SPI supports two modes of the Motorola standard.
The iC-MCW samples MOSI on rising edges of SCLK and generates data on falling edges of SCLK. The corresponding Motorola modes that can be used by the SPI master of the host system are:

CPOL = 0, CPHA = 0
CPOL = 1, CPHA = 1

The data lengths of opcodes, addresses and registers are 8 bit. All data is sent MSB first. Continuous register access and BiSS frame data are transmitted serially in successive byte chunks.
The chip select line NCS is low active. It starts a new SPI transmission on the falling edge and cancels any SPI transmission on the rising edge.
The idle state of SCLK is not determined.

SPI Commands

Each SPI transmission starts with an opcode sent from the host system to the SPI slave via MOSI. The four available commands and the corresponding opcodes are listed in Table 11.

Opcode	Command
0x9C	Read Status
0xA6	Read Frame Data
0x8A	Read Register
0xD2	Write Register

Table 11: SPI Commands

Invalid SPI opcodes trigger an error that is reported to the error pin ERR. The SPI error bit must be reset manually with the SPI command Write Register.

SPI Command: Read Status (0x9C)

The SPI command Read Status triggers the iC-MCW to latch the STATUS Byte that can be clocked out of MISO. The first byte of MOSI is the command's opcode 0x9C and the second byte of MISO shows the latched status information. An example of the Read Status transmission can be found in Figure 8.

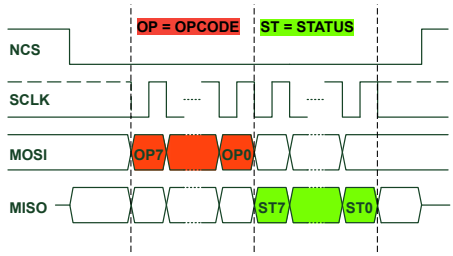

Figure 8: SPI Transmission Read Status (0x9C)

The command Read Status is intended for applications that do not use interrupt- driven I/O to manage the communication.

STATUS Byte

The STATUS Byte is composed of several bits from the registers DeviceStatus and DeviceError as shown in Table 12. More information about iC-MCW's registers can be found in chapter REGISTER LAYOUT on page 10.

STATUS								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	AVAIL	DETECT	WAIT		PLL	SPI	FRAME	RST

Table 12: STATUS Byte of SPI Command Read Status

All error bits of register DeviceError (PLL, SPI, FRAME and RST) are connected to the OR-gate of iC-MCW's error pin ERR to externally inform the host system about any unusual behaviour.

The error bits of DeviceError are persistent and must be reset manually by sending the SPI command Write Register to this register.

STATUS Byte: AVAIL and DETECT

AVAIL and DETECT are used to inform the host about new frame data for communication systems that use status polling instead of interrupt requests via pin IRQ. The bit AVAIL reports new frame data is ready to be transmitted to the host. The bit DETECT is set as soon as a BiSS timeout is detected by the iC-MCW. DETECT is cleared together with the frame counter if the SPI command Read Frame Data is successfully executed. If the bit DETECT is set but AVAIL equals zero, the currently activated RAM bank is busy and cannot be addressed to access the received frame data.

AVAIL	Addr. 0x01; bit 4	R
Code	Description	
0	No Frame Data Available	
1	New Frame Data Available	

Table 13: Availability of new Frame Data

DETECT	Addr. 0x01; bit 3	R
Code	Description	
0	No BiSS Frame Detected	
1	New BiSS Frame Detected	

Table 14: Detection of a new BiSS Frame

STATUS Byte: WAIT

WAIT shows the waiting state of iC-MCW that are sent as part of the STATUS Byte. The waiting state can be used to monitor what signal the iC-MCW is waiting for. This information allows debugging the communication if the chip waits for the start bit an exceptional period of time for example.

WAIT can be mapped to the internal system states as shown in Table 15. Detailed information about the in-

ternal system states STATE can be found in chapter MODE OF OPERATION on page 12.

WAIT		
Code	Current System State	Task
0b00	IDLE	Wait for Begin of Frame
0b01	DELAY	Wait for Acknowledge
0b10	START	Wait for Start Bit
0b11	ABTO, READY, CDS, DATA or ERROR	Wait for BiSS Timeout

Table 15: Waiting States transmitted in STATUS Byte

STATUS Byte: PLL

PLL corresponds to the error bit of the register DeviceError directly. It is set to indicate an issue with the internal PLL.

PLL	Addr. 0x02; bit 6	R/W
Code	Description	
0	PLL Lock OK	
1	PLL Lock Warning	

Table 16: PLL Lock Status

STATUS Byte: SPI

The bit SPI combines the bits OPCODE, READ and WRITE. SPI is asserted if one of the corresponding error bits is set.

SPI	
Code	Description
0	SPI Communication OK
1	SPI Communication Error. One of the error bits OPCODE, READ and WRITE is set.

Table 17: SPI Communication Status

OPCODE	Addr. 0x02; bit 4	R/W
Code	Description	
0	SPI Opcode valid	
1	SPI Opcode invalid	

Table 18: SPI Opcode validity

READ	Addr. 0x02; bit 3	R/W
Code	Description	
0	SPI Read Address valid	
1	SPI Read Address invalid	

Table 19: SPI Read Address validity

WRITE	Addr. 0x02; bit 2	R/W
Code	Description	
0	SPI Write Address valid	
1	SPI Write Address invalid	

Table 20: SPI Write address validity

STATUS Byte: FRAME

The bit FRAME indicates that there is an issue with the BiSS protocol. It combines the bits SFRAME and HFRAME and is asserted if one of the corresponding error bits is set.

SFRAME indicates a soft error and is set if a LENGTH_ERROR occurs (INFO=0xFB) or the SLI warning is active (WARN=1). HFRAME indicates a hard error and is set when no BiSS data could be processed. The root cause of the indicated error in HFRAME is described in CODE.

FRAME	
Code	Description
0	Frame Data OK.
1	Frame Error Detected. One of the error bits SFRAME or HFRAME is set.

Table 21: Frame Status

SFRAME	Addr. 0x02; bit 7	R/W
Code	Description	
0	No BiSS Frame Soft Error Detected.	
1	BiSS Frame Soft Error Detected. INFO=0xFB or WARN=1 are the root cause.	

Table 22: Soft Frame Error

HFRAME	Addr. 0x02; bit 1	R/W
Code	Description	
0	No BiSS Frame Hard Error Detected.	
1	BiSS Frame Hard Error Detected. See CODE for root cause.	

Table 23: Hard Frame Error

Further information about the register DeviceError can be found in section REGISTER LAYOUT on page 10.

STATUS Byte: RST

RST indicates a chip reset.

RST	Addr. 0x02; bit 0	R/W
Code	Description	
0	No Chip Reset Detected	
1	Chip Reset Detected	

Table 24: Chip Reset Detection

SPI Command: Read Frame Data (0xA6)

In general the command Read Frame Data provides a continuous stream of bytes of the last completely processed BiSS frame. The command should only be used if an interrupt request is detected at pin IRQ by the host system or the bit AVAIL of the STATUS Byte is set.
After receiving the opcode 0xA6 in the first byte on pin MOSI, the iC-MCW returns the byte INFO that reports the status of the current BiSS frame in the second byte on pin MISO. There are several codes of INFO that indicate what data is provided in the following SPI bytes. Table 25 describes the possible output of INFO.

INFO Byte

The INFO Byte holds the number of data bytes of the current BiSS frame. If there is no valid frame data available, the INFO code can be used for debugging. The INFO Byte matches the register FrameInformation in Table 7.

INFO	Addr. 0x03; bit 7:0	R
Code	Name	Description
0x00	NO_DATA	Valid BiSS Frame, CDS and NCDM only
0x01 . . . 0xFA	FRAME_LENGTH	Valid BiSS Frame, Data Ready to Transmit
0xFB	LENGTH_ERROR	Incomplete BiSS Frame Data, only 250 Bits available
0xFC	NO_CDS	Reduced BiSS Frame Detected, NCDM only
0xFD	FRAME_ERROR	BiSS Frame Error, see error code
0xFE	BANK_BUSY	Memory Bank busy, Data invalid
0xFF	NO_FRAME	No BiSS Frame in memory

Table 25: INFO Byte of SPI Command Read Frame Data

INFO Byte: NO_DATA

A short BiSS frame does not transmit any sensor data to the slave. If the iC-MCW detects a BiSS timeout directly after the CDS bit has been sampled, the byte INFO is set to NO_DATA. There are no further data bytes that need to be clocked out of pin MISO.

INFO Byte: FRAME_LENGTH

FRAME_LENGTH shows the valid frame length of the current BiSS frame in memory. The value of INFO must be used to calculate the number of frame data bytes that need to be clocked out of MISO to completely transmit the available frame data.
Since the frame data is shifted from the LSB to the MSB of each memory cell and the number of sampled bits does not naturally match the number of configured frame bits, the last byte must possibly be masked to accurately extract the data bits. The difference of the expected BiSS frame length and the sampled frame length reported by FRAME_LENGTH can be used to identify the actual BiSS frame bits of the last byte. Figure 9 shows the position of the frame bits within the last data byte to help calculating the valid frame data.

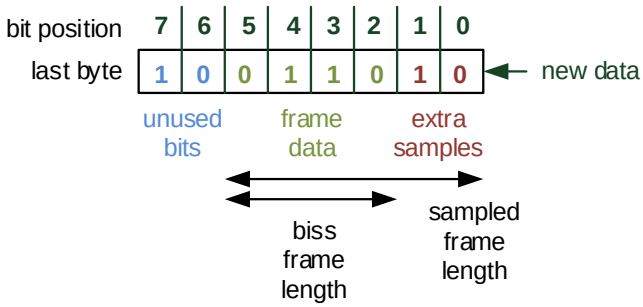

Figure 9: Last Data Byte

INFO Byte: LENGTH_ERROR

The iC-MCW is capable of capturing BiSS frames of up to 250 bits including CRC protection. If the BiSS engine detects a valid communication of 251 bits and above, the byte INFO shows LENGTH_ERROR and the following 32 bytes can be clocked out to transmit 250 bits of the processed BiSS frame. However, the BiSS communication is not completely available and must be handled as a communication error.

INFO Byte: NO_CDS

The reduced BiSS frame only sends the NCDM bit from the BiSS master to the BiSS slave. Since there is no sensor data transmitted, there are no further frame data bytes to be clocked out of pin MISO.

INFO Byte: FRAME_ERROR

FRAME_ERROR indicates a BiSS Protocol error during frame processing. The register FrameError is sent on MISO in the third byte and can be used to debug communication. FrameError contains CODE and WARN. The two bits CODE represent the type of the BiSS Protocol Hard Error HFRAME and the bit WARN represents the type of the BiSS Protocol Soft Error SFRAME. WARN is set if the BiSS data line SLI was digital low at the beginning of the current BiSS frame.

CODE	Addr. 0x06; bit 2:1	R
Code	Type (STATE)	Description
0b00	Timeout (ABTO)	Timeout during Measurement of adaptive BiSS Timeout
0b01	Timeout (START)	Timeout during Start Bit execution
0b10	Timeout (CDS)	Timeout during CDS execution
0b11	Level (DELAY)	SLI level error during Line Delay measurement

Table 26: BiSS Frame Hard Error Type

WARN	Addr. 0x06; bit 0	R
Code	Description	
0	No Warning.	
1	BiSS data line SLI was digital low at the beginning of the current BiSS frame.	

Table 27: BiSS Frame Soft Error Type

INFO Byte: BANK_BUSY
If the current read bank has already been read out and a new incoming frame is still in progress, iC-MCW did not have the chance to switch the memory bank. Thus, the bank is considered to be busy and INFO equals BANK_BUSY to report an invalid data access. Hence, there is no frame data to be read out of the memory of the iC-MCW.

In general, it is recommended to only send a Read Frame Data command if an interrupt request signal at pin IRQ is detected or the bit AVAIL is set.

INFO Byte: NO_FRAME
If INFO equals NO_FRAME, there was no new frame detected since the last Read Frame Data command. Hence, there is no frame data to be read out of the memory of the iC-MCW.

Optional Bytes
At the end of the SPI command Read Frame Data, there are several optional bytes that contain additional information of the BiSS communication.
The first two bytes contain the control data bits CDS and NCDM as well as the number of the current frame FNUM the host reads the data of. The 14-bit frame number is sent MSB first and begins after the bits CDS and NCDM are clocked out. It holds the current index of the frame that can be used for verifying the sign-of-life-counter of the BiSS frame and the CDS and NCDM bits of the BiSS C Control Data communication.

CDS	Addr. 0x05; bit 7	R
Code	Description	
0	CDS = 0	
1	CDS = 1	

Table 28: CDS Bit

NCDM	Addr. 0x05; bit 6	R
Code	Description	
0	CDM = 1	
1	CDM = 0	

Table 29: Inverted CDM Bit

FNUM	Addr. 0x04, bit 7:0; Addr 0x05, bit 5:0	R
Code	Description	
0x0000 ... 0x3FFF	Number of lost BiSS Frames during last SPI access	

Table 30: Frame Number

The first two optional bytes match the frame information available in register FrameNumberCD.
The next four bytes contain the registers BiSS Measurement that can be used to analyze the BiSS communication in general.

P_TIME	Addr. 0x0D, bit 7; Addr 0x0F, bit 7:0	R
Code	Description	
0x000 ... 0x1FF	Processing time in clock periods T_MA	

Table 31: BiSS Frame Processing Time

L_DELAY	Addr. 0x0D, bit 7:5; Addr 0x0E, bit 6:0	R
Code	Description	
0x000 ... 0x3FF	Line Delay in sample periods $T_{\_SMP}$	

Table 32: BiSS Frame Line Delay

C_TIME	Addr. 0x0C, bit 7:0; Addr 0x0D, bit 4:0	R
Code	Description	
0x0000 ... 0x1FFF	Cycle Time in sample periods $T_{\_SMP} \cdot 2^5$	

Table 33: BiSS Frame Cycle Time

P_TIME (9 Bit) can be used to detect differences regarding the delay of the start bit. Since it is measured in full MA clocks, the maximum processing time depends on the chosen BiSS frequency.
L_DELAY (10 Bit) represents the time between the second rising edge of MA and the first falling edge of SL. It is measured in sample periods which is the highest accuracy possible.
C_TIME (13 Bit) is intended to observe the first rising

edge of MA on which the data is latched within the sensor. The value shows the time in between the current and the last frame. Its resolution is the sample period multiplied by 2^5 to support BiSS frames configured to large cycle times.

Since the sample period depends on the system clock, the BiSS measurement parameters can only be compared over time to detect any erroneous behavior.

More information about the registers BiSS measurement can be found in REGISTER LAYOUT on page 10.

Figure 10 illustrates the sequence of a Read Frame Data command with INFO = FRAME_LENGTH and transmission of the optional control data (CDS, NCDM), frame number (FNUM) and BiSS Measurement (P_TIME, L_DELAY, C_TIME).

Since the SPI command Read Frame Data always resets the frame counter, the optional bytes should always be clocked out to correctly calculate the sign-of-life counter. Except for INFO = NO_FRAME, the frame counter is always available after the frame data or error byte is read. Especially INFO = NO_CDS and INFO = NO_DATA need to clock out the byte that contains the bits CDS and NCDM for the BiSS control communication.

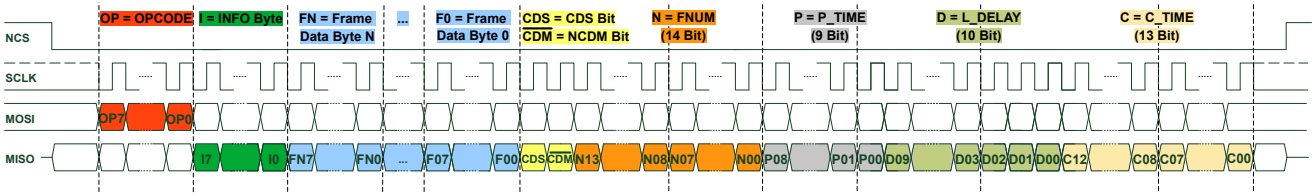

Figure 10: SPI Transmission Read Frame Data (0xA6)

SPI Command: Read Register (0x8A)

The command Read Register is used to read an address of the register bank shown in Table 7 of chapter REGISTER LAYOUT on page 10.
The first byte of MOSI is the opcode 0x8A and the second byte is the desired register address. While transmitting the register address, the pin MISO clocks out the STATUS Byte. The third byte contains the data of the register that was selected by the address byte.

Additional bytes activate the continuous read function. The iC-MCW increments the register address automatically and multiple registers can be read with one single SPI transmission.
Invalid register addresses trigger an SPI error that is reported to the error pin ERR and the register DeviceError. The SPI error bit must be reset manually.
Figure 11 shows an example of the Read Register transmission.

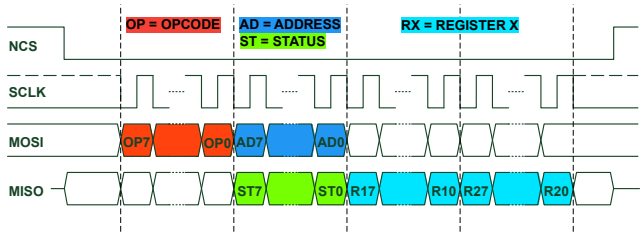

Figure 11: SPI Transmission Read Register (0x8A)

SPI Command: Write Register (0xD2)

The command Write Register is used to write an address of the register bank shown in REGISTER LAYOUT on page 10.
The first byte of MOSI is the opcode 0xD2 and the second byte is the desired register address. While transmitting the register address, the pin MISO clocks out the STATUS Byte. The third byte contains the data to be written to the register that was selected by the address byte.
In contrast to the command Read Register, there is no continuous write function implemented.
Since the iC-MCW does not need any configuration, the command Write Register is exclusively used to reset the error bits in the register DeviceError. If the SPI engine recognizes a write access to the register DeviceError, the error bits are reset no matter what the

write data of the SPI opcode Write Register is.
Invalid register addresses and register addresses that are read-only trigger an SPI error that is reported to the error pin ERR and the register DeviceError. The SPI error bit must be reset manually.
Figure 12 shows an example of the Write Register transmission.

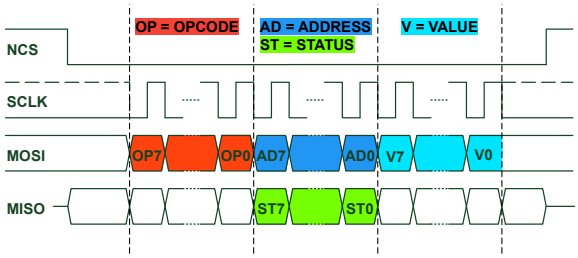

Figure 12: SPI Transmission Write Register (0xD2)

DESIGN REVIEW

iC-MCW_Z1		
No.	Function, Parameter/Code	Description and Application Notes
1	Frame Error	The frame error in register DeviceError is not divided into SFRAME and HFRAME. Instead, both error types are indicated as HFRAME. See section DeviceError for further information.
2	BiSS Measurement	The BiSS Measurement is not implemented. The parameter C_TIME, L_DELAY and P_TIME are neither accessible via SPI command Read Frame Data nor available in the BiSS Measurement registers.
3	RS422 BiSS Interface	Short BiSS idle pulses < 100 ns at MA have to be prevented. Thus, a maximum frequency fclk(MA) (El.Char. B08) of 5 MHz should not be exceeded. It is recommended to place iC-MCW as close as possible to the BiSS master to comply with above mentioned timing requirements. The threshold voltages Vt()hi (El. Char. B05) and Vt()lo (El. Char. B06) at MA/NMA and SL/NSL depend on the BiSS clock frequency fclk(MA) at MA. The following signal levels at iC-MCW's receiver are required in order to ensure proper function with respect to the applied BiSS clock frequency. 100 kHz $<$ fclk(MA) $\leq$ 5 MHz: |Vdiff(MA)| = |V(MA)-V(NMA)| > 400 mV, |Vdiff(SL)| = |V(SL)-V(NSL)| > 300 mV fclk(MA) $\leq$ 100 kHz: |Vdiff(MA)| = |Vdiff(SL)| = 200 mV (as stated in El. Char. B05 and B06)
4	NCDM	NCDM does not state the current inverted CDM value but is always "0".

Table 34: Notes on Chip Functions Regarding the Chip Release of iC-MCW_Z1

iC-MCW_Y		
No.	Function, Parameter/Code	Description and Application Notes
1	RS422 BiSS Interface	Short BiSS idle pulses < 100 ns at MA have to be prevented. Thus, a maximum frequency fclk(MA) (El.Char. B08) of 5 MHz should not be exceeded. It is recommended to place iC-MCW as close as possible to the BiSS master to comply with above mentioned timing requirements. The threshold voltages Vt()hi (El. Char. B05) and Vt()lo (El. Char. B06) at MA/NMA and SL/NSL depend on the BiSS clock frequency fclk(MA) at MA. The following signal levels at iC-MCW's receiver are required in order to ensure proper function with respect to the applied BiSS clock frequency. 100 kHz $<$ fclk(MA) $\leq$ 5 MHz: |Vdiff(MA)| = |V(MA)-V(NMA)| > 400 mV, |Vdiff(SL)| = |V(SL)-V(NSL)| > 300 mV fclk(MA) $\leq$ 100 kHz: |Vdiff(MA)| = |Vdiff(SL)| = 200 mV (as stated in El. Char. B05 and B06)
2	NCDM	NCDM does not state the current inverted CDM value but is always "0".

Table 35: Notes on Chip Functions Regarding the Chip Release of iC-MCW_Y

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2018-01-18	All	Initial Release	All

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2020-10-21	FEATURES	Added "Analysis Data of BiSS Protocol" for BiSS Measurement Functions.	1
		THERMAL DATA	Fixed Standard Operating Ambient Temperature Range. Moved Storage Temperature to THERMAL DATA.	5
		ELECTRICAL CHARACTERISTICS	Adapted specification of Vt()lo (El. Char. B06). Adapted specification of Power-On-Reset.	6f
		REGISTER LAYOUT	Split "FRAME" Error Bit into SFRAME and HFRAME. Removed "Byte" Error Bit from Register "DeviceError". Removed "FrameCounter" from the Register Layout (accessible parameter: FNUM). Added BiSS Measurements P_TIME, L_DELAY and C_TIME to the Register Layout. Removed irrelevant Chip Revisions from CHIP_REV. Moved relevant parameter information from REGISTER LAYOUT to corresponding sections in HOST INTERFACE.	10f
		ELECTRICAL CONNECTIONS	Added Note for Ground Connections.	11
		START-UP	Added Note in "Power On Reset". Added section "BiSS Measurement: Cycle Time". Removed section "BiSS Input".	12
		MODE OF OPERATION	Renamed "Long Frame" to "Standard Frame".	12ff
		HOST INTERFACE	Added BiSS Measurement P_TIME, L_DELAY and C_TIME.	16ff

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2021-06-25	All	Removed "Preliminary"	All
		REGISTER LAYOUT	Added note for RESERVED registers 0x07...0x0B.	10
		MODE OF OPERATION	Added info about maximum value of FNUM.	15
		HOST INTERFACE	Updated Figures for SPI Transmissions. Updated description of HFRAME and SFRAME.	17ff
		DESIGN REVIEW	Updated design review for RS422 BiSS Interface Added design review for NCDM	23

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MCW	24-pin QFN24, 4 mm x 4 mm, thickness 0.9 mm, RoHS compliant	iC-MCW QFN24-4x4
Evaluation Board	80 mm x 100 mm eval board	iC-MCW EVAL MCW1D

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