iC-PE Series

XMR SENSOR MULTIPLEXER-AMPLIFIER

preliminary

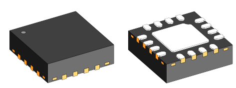
FEATURES

- Differential 3:1 channel analog multiplexer
- Internal shift register for chain operation of multiple devices
- Implemented safety protocol
- Sensor reading activated by serial data
- Differential gain 1, 10, 20, 30, 50
- 3-channel differential rail-to-rail inputs
- Channel settling < 25 µs after selection
- Input bias current < 1 nA
- Internal offset-canceling function
- 1-channel differential rail-to-rail output, bus-capable
- Output current capability 1 mA, short-circuit-proof
- 3 V to 5.5 V supply voltage
- Current consumption < 100 µA during 3.3 V operation
- Standby current < 15 µA at 3.3 V
- Operating temperature range of -40 °C to +125 °C

APPLICATIONS

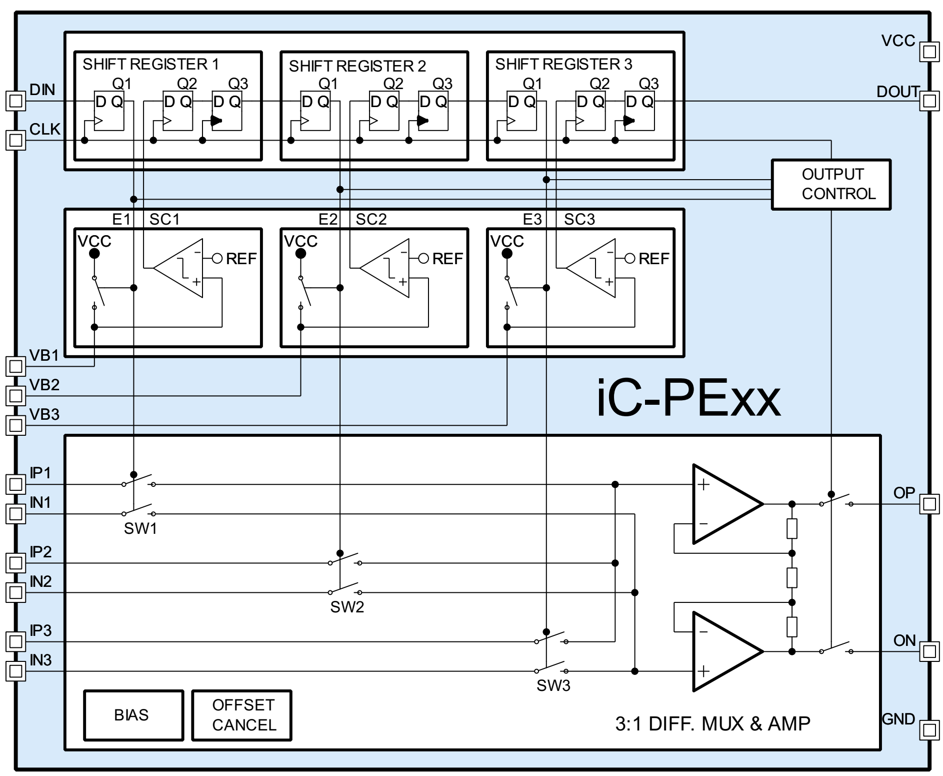
- AMR, GMR, TMR sensor conditioning
- Magnetic Field Sensing
- Proximity Switches
- Position Sensors
- Safety Applications

PACKAGES



QFN16
3 mm x 3 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-PExx* is a low-power 3:1 multiplexed amplifier with differential rail-to-rail inputs and outputs. Its internal shift register allows sequential reading of 3 sensors per chip.

Multiple chips can be connected in chain configuration, permitting the reading of a large number of sensors, minimizing bill-of-materials and system power consumption.

Besides the multiplexer and amplifier function, the iC-PExx features a sensor supply control. The circuit and the sensor supply outputs are activated by serial data, making iC-PExx especially suited for power sensitive applications.

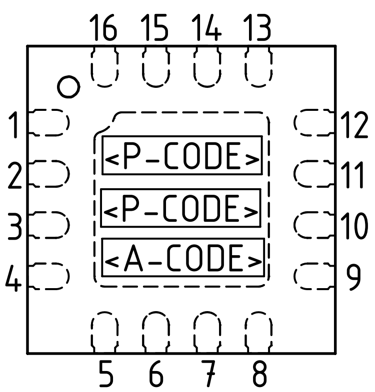
By means of the implemented safety protocol, sequential reading is interrupted when a short-circuit condition is detected. In the same way, iC-PExx provides short-circuit protected outputs.

For precision applications, iC-PExx features internal offset canceling function and low-noise performance.

*) xx = device version, depending on GAIN.

PACKAGING INFORMATION

PIN CONFIGURATION
QFN16 3 mm x 3 mm (top view)

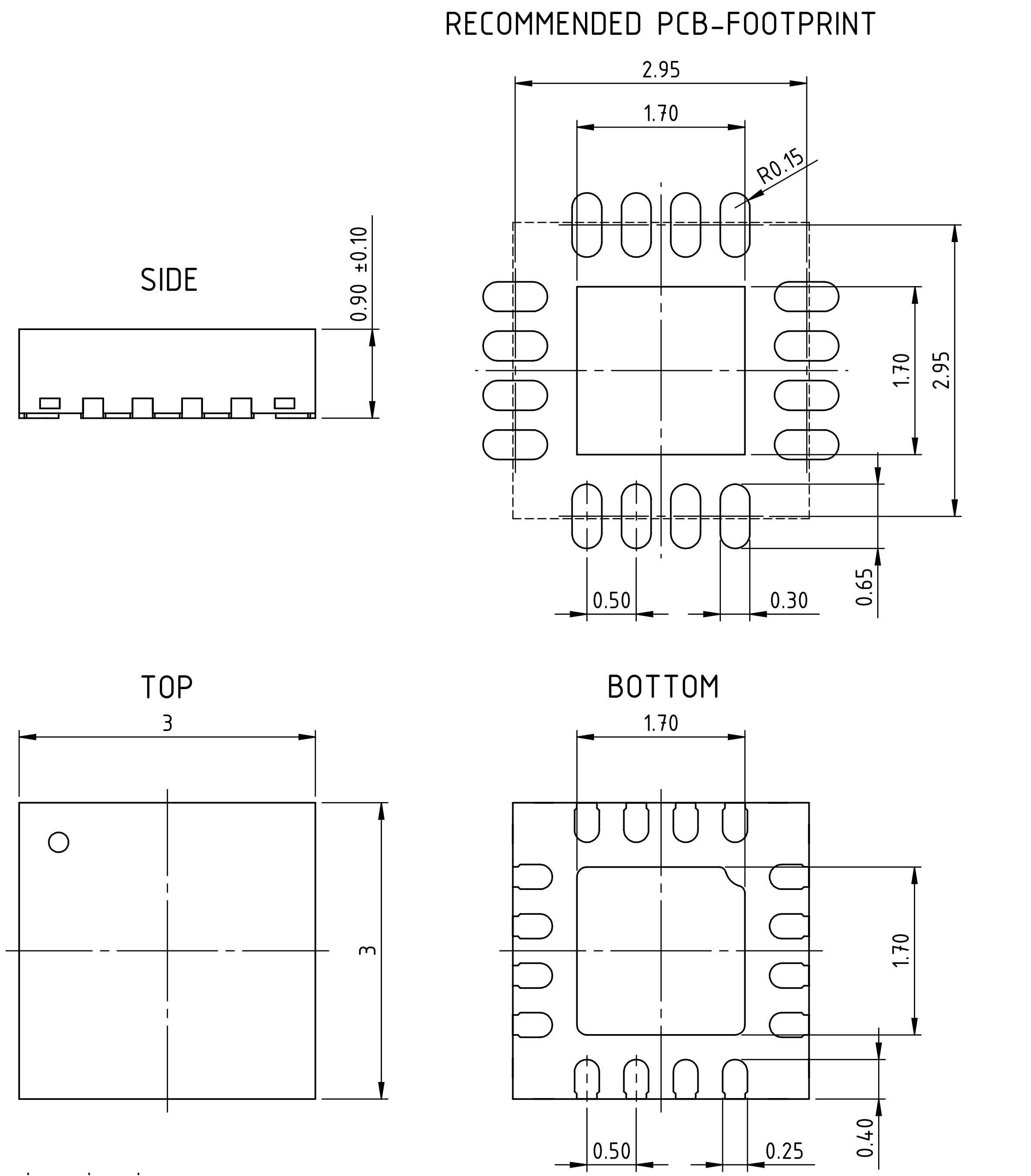


PIN FUNCTIONS

No.	Name	Function
1	IP1	Sensor Input 1
2	VB1	Sensor Supply Output 1
3	DIN	Control Logic, Data Input
4	CLK	Control Logic, Clock Input
5	GND	Ground
6	OP	Analog Output
7	ON	Analog Output, inverted
8	VCC	+3.0 V...+5.5 V Supply Voltage Input
9	DOUT	Control Logic, Data Output
10	IN3	Sensor Input 3, inverted
11	IP3	Sensor Input 3
12	VB3	Sensor Supply Output 3
13	IN2	Sensor Input 2, inverted
14	IP2	Sensor Input 2
15	VB2	Sensor Supply Output 2
16	IN1	Sensor Input 1, inverted
	BP [1)]	Backside Paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

drb_qfn16-3x3-1_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.5	6	V
G002	I(VCC)	Current in VCC		-10	80	mA
G003	V()	Voltage at IPx, INx		-0.5	VCC + 0.5	V
G004	I()	Current in IPx, INx		-5	5	mA
G005	V()	Voltage at Ox		-0.5	6	V
G006	I()	Current in Ox		-30	30	mA
G007	V()	Voltage at VBx		-0.5	6	V
G008	I()	Current in VBx		-10	10	mA
G009	Vdiff()	Differential Voltage at IPx vs. INx		-6	6	V
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		1	kV
G011	Tj	Chip Temperature		-40	150	ºC
G012	Ts	Storage Temperature		-40	150	ºC

THERMAL DATA

Operation Conditions: VCC = 3.0 V to 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	ºC
T02	Rthja	Thermal Resistance Chip to Ambient	QFN16-3x3 surface mounted to PCB according to JEDEC 51 thermal measurement standards		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 3.0 V to 5.5 V, Tj = -40...125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VCC	Permissible Supply Voltage		3		5.5	V
002	I(VCC)	Supply Current in VCC	VCC active, after CLK lo → hi with DIN pulse Logic inputs below 0.1 VCC or above 0.9 VCC; VCC = 3 V, without load VCC = 5.5 V, without load			 80 160	 µA µA
003	I(VCC)	Standby Current in VCC	VCC active, before CLK lo → hi with DIN pulse and/or after DOUT lo → hi transition Logic inputs below 0.1 VCC or above 0.9 VCC; VCC = 3 V, without load VCC = 5.5 V, without load			 12.5 25	 µA µA
004	Vc()hi	Clamp Voltage hi at OP, ON, VBx	VCC = 0 V, I() = 10 mA	0.3		1.65	V
005	Vc()lo	Clamp Voltage lo at OP, ON, VBx	VCC = 0 V, I() = -10 mA	-1.65		-0.3	V
006	Vc()hi	Clamp Voltage hi at IPx, INx, CLK, DIN, DOUT	VCC = 0 V, I() = 1 mA	0.3		1.65	V
007	Vc()lo	Clamp Voltage lo at IPx, INx, CLK, DIN, DOUT	VCC = 0 V, I() = -1 mA	-1.65		-0.3	V
008	G	Differential Gain PE01	(OP - ON) / (IP - IN), measured with IP - IN = 1 V, Vcm = 1/2 VCC		1		V/V
009	G	Differential Gain PE10	(OP - ON) / (IP - IN), measured with IP - IN = 100 mV, Vcm = 1/2 VCC		10		V/V
010	G	Differential Gain PE20	(OP - ON) / (IP - IN), measured with IP - IN = 50 mV, Vcm = 1/2 VCC		20		V/V
011	G	Differential Gain PE30	(OP - ON) / (IP - IN), measured with IP - IN = 33 mV, Vcm = 1/2 VCC		30		V/V
012	G	Differential Gain PE50	(OP - ON) / (IP - IN), measured with IP - IN = 20 mV, Vcm = 1/2 VCC		50		V/V
013	Gerr	Differential Gain Error	measured with Vcm =1/2 VCC			10	%G
Analog Input Ports: IP1...3, IN1...3							
101	Vcm()	Permissible Input Voltage Range		0		VCC	V
102	Vos	Input Offset Voltage	Vcm = 1/2 VCC, RL > 100 kΩ measured during Offset-Free state, 40 µs after CLK lo → hi			1.5	mV
103	Iin()	Input Leakage Current	V(IPx, INx) = 0..VCC	-1		1	nA
104	Ios()	Input Offset Current |Iin(IPx)-Iin(INx)|	V(IPx, INx) = 0..VCC	-1		1	nA
105	Vnoise	Input Referred Noise Voltage	integrated over 1 MHz bandwidth		200		µVpp
Analog Outputs: OP, ON							
201	V()hi	Output Voltage hi	V()hi = VCC - V(), RL = 100 kΩ vs. GND			200	mV
202	V()lo	Output Voltage lo	RL = 100 kΩ vs. VCC			200	mV
203	Vs()hi	Saturation Voltage hi	Vs()hi = VCC - V(), I() = -1 mA Tj = 27 °C Tj = 125 °C			 800 1000	 mV mV
204	Vs()lo	Saturation Voltage lo	I() = 1 mA Tj = 27 °C Tj = 125 °C			 400 500	 mV mV
205	Isc()hi	Short-Circuit Current hi	short to GND	-9		-2	mA
206	Isc()lo	Short-Circuit Current lo	short to VCC	2		9	mA
207	Vcmo	Output Common-Mode Voltage	RL = 100 kΩ Vcmo tracks input common-mode	100		VCC - 100	mV
208	tset	Settling Time	after E(x) lo → hi, to 99 % of steady-state value; IP = IN, 0 to VCC/2 step, CL = 40 pF, RL = 24 kΩ IP = IN, 0 to VCC/2 step, CL = 100 pF, RL =10 kΩ			 25 40	 µs µs

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 3.0 V to 5.5 V, Tj = -40...125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Sensor Supply Outputs: VB1...3							
301	Vout()	Output Voltage	VCC = 3 V, RL = 10 kΩ vs. GND VCC = 5 V, RL = 10 kΩ vs. GND	2.92 4.92		2.99 4.99	V V
302	Vdiff()	Maximum Voltage Difference	between VBx pins			1	%
303	Isc()hi	Short-Circuit Current	short to GND; VCC = 3 V VCC = 5 V	-15 -25		-7.5 -12.5	mA mA
Dynamic Parameters							
401	UGBW	Unity-Gain Bandwidth	Vcm = 1/2 VCC, RL > 100 kΩ, CL < 15 pF measured during offset learning state		200		kHz
402	Fmax	Maximum Clock Frequency	CLK duty cycle = 50%, CL < 15 pF required to avoid settling-time or offset-learning errors			25	kHz
Control Logic: Inputs DIN, CLK							
501	Vt()hi	Threshold Voltage hi				78	%VCC
502	Vt()lo	Threshold Voltage lo		22			%VCC
503	Vhys()	Schmitt-Trigger Input Hysteresis		100			mV
504	Ipd()	Pull-down Current				10	µA
Control Logic: Output DOUT							
601	Vs()hi	Saturation Voltage hi	Vs()hi = VCC - V(DOUT), I() = -4 mA; Tj = 27 °C Tj = 125 °C			 0.7 1	 V V
602	Vs()lo	Saturation Voltage lo	I() = 4 mA; Tj = 27 °C Tj = 125 °C			 0.7 1	 V V
603	Isc()hi	Short-Circuit Current hi	V() = 0 V, Tj = 27 °C	-50			mA
604	Isc()lo	Short-Circuit Current lo	V() = VCC, Tj = 27 °C			50	mA
605	tr()	Rise Time	CL() = 50 pF, Tj = 27 °C			100	ns
606	tf()	Fall Time	CL() = 50 pF, Tj = 27 °C			100	ns

OPERATING REQUIREMENTS: Control Logic

Operating conditions: VCC = 3.0 V to 5.5 V, Tj = -40...125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Control Logic						
I001	tset	Setup Time	DIN stable before CLK lo → hi		50	ns
I002	thold	Hold Time	DIN stable after CLK lo → hi		50	ns
I003	telh	Channel Enable Time	E1-3 lo → hi after CLK lo → hi		50	ns
I004	tehl	Channel Disable Time	E1-3 hi → lo after CLK lo → hi		50	ns
I005	tplh	Propagation Time	DOUT lo → hi after CLK hi → lo		50	ns
I006	thl	Propagation Time	DOUT hi → lo after CLK hi → lo		50	ns

Operating Modes

In iC-PE30, both sensor reading and chip power consumption is controlled by serial data. In terms of power, it has two different operation modes, Standby and Active. As long as the chip gets a valid supply voltage (VCC minimum value is 3 V), it enters Standby Mode, drawing a small current (typ. below 10 µA at 3.3 V).

When a DIN pulse is captured by the CLK signal, the chip enters Active Mode, performing a serial reading of all 3 differential channels with a modest power consumption (typ. below 100 µA at 3.3 V). After DOUT pulse generation, the chip gets back to Standby Mode. This behavior is shown in Figure 1.

State Sequences

iC-PExx is activated by serial data. After DIN pulse is captured by the CLK signal, the three channels E1-3 are enabled and disabled sequentially as shown in Figure 1. The reading time for each channel has a duration of two CLK cycles. During channel reading, a sequence of 4 states is followed.

State1 (offset learning): the amplifier is working normally (OP - ON = G (IP - IN), with G = 1, 10, 20, 30 or 50). In this state, the amplifier may present some offset Voff which will also be amplified together with the input signal. For this reason, the system will simultaneously learn this offset for a subsequent substraction in State3.

State2 (transition): during this state the outputs OP, ON are disconnected (left in high-impedance: Hz).

State3 (offset free): in this state the amplifier works normally again, but offset has been removed.

Finally, in State4 the outputs OP, ON are disconnected again, as in State2. Note that State4 serves as a guard-time to avoid any time overlap between channels.

The sequence of states 1 to 4 is repeated for each channel. Apart from States 1 and 3, the outputs are always in high-impedance (disconnected), so that multiple iC-PExx's can be connected to the same bus in chain operation. After finishing reading the 3 channels, a DOUT pulse is generated. In a chain connection (refer to Figure 4), DOUT controls DIN of the next iC-PExx in the chain.

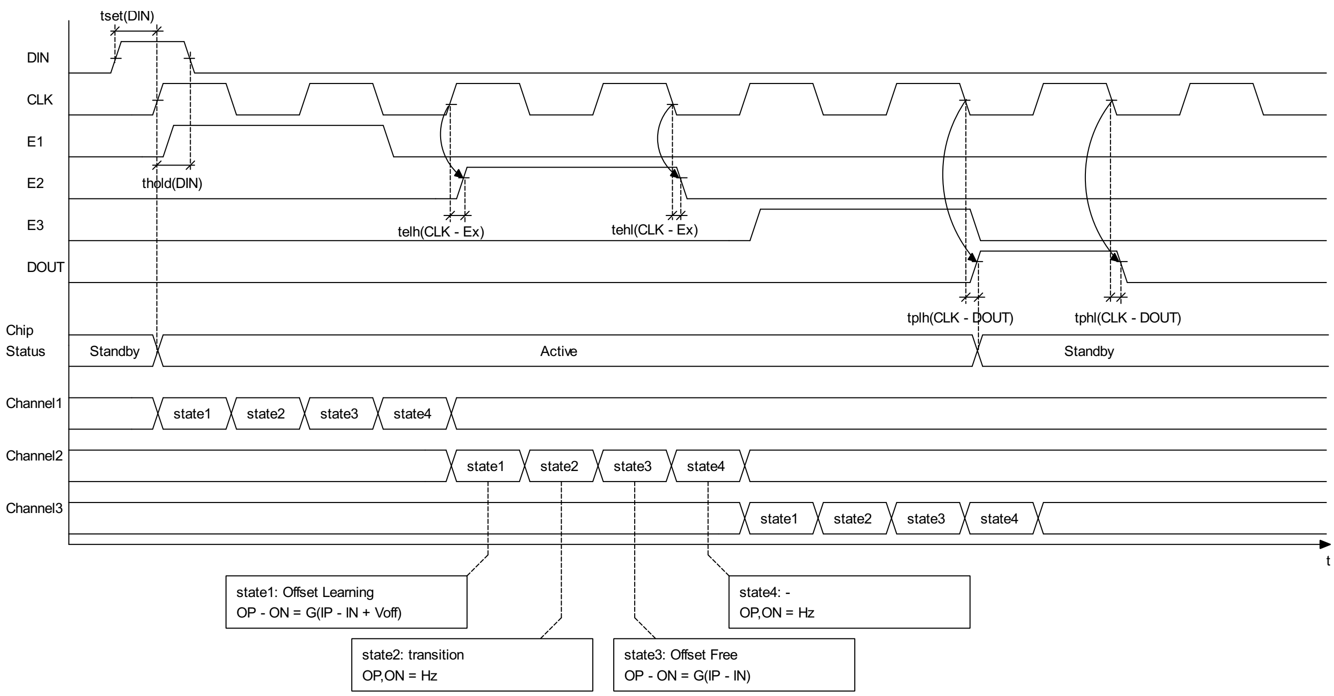


Figure 1: Timing characteristics

OPERATING REQUIREMENTS: Internal Offset Canceling Function

Operating conditions: VCC = 3.0 V to 5.5 V, Tj = -40...125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Internal Offset Canceling Function						
I101	tmin	Minimum Sampling Time for Internal Offset Canceling Function CLK hi	Cload < 100 pF	20		µs
I102	toc	Offset Canceling Availability	after CLK hi → lo, T < 85 °C		500	ms

The iC-PExx internal offset canceling allows offset-free readings during a limited amount of time. A set of timing constraints applies here. There is a minimum time (tmin) in State1 in order to guarantee that the amplifier's offset has been properly read and stored. Also, due to internal leakage currents, the offset cancelation in State3 is operative only during a given amount of time (toc). It must be noted that during offset learning (State1) the system is operative. Therefore, iC-PExx can be used without internal offset canceling and without any timing restrictions just considering State1 if desired.

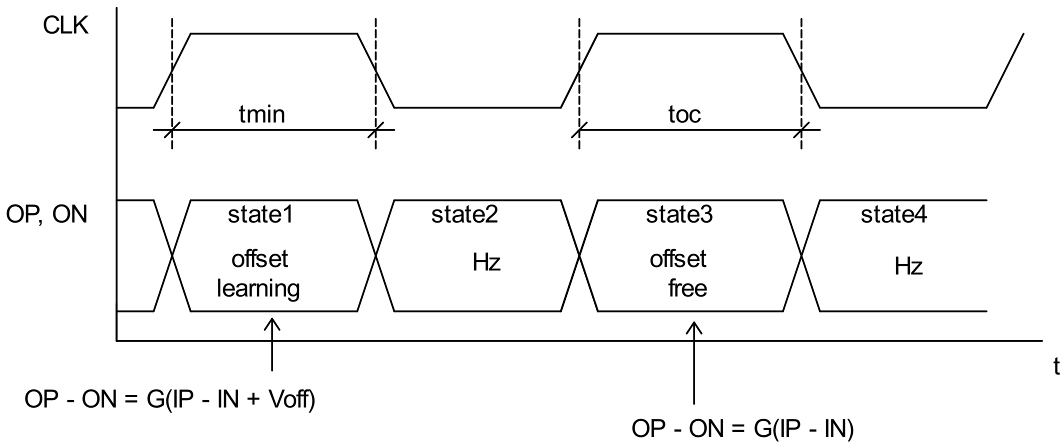


Figure 2: Internal offset canceling function timing characteristics

APPLICATION EXAMPLES

The iC-PExx performs sequential reading of 3 sensors per chip. Combined with magnetoresistive sensors, such as TMR, this allows measuring 3-axis magnetic field with a single chip, leading to an excellent solution for vehicle detection or parking sensor application.

iC-PExx can be also connected in chain configuration, allowing sequential reading of a large number of sensors. This option is suitable for magnetic scanning applications, like NDT (non-destructive test), among others.

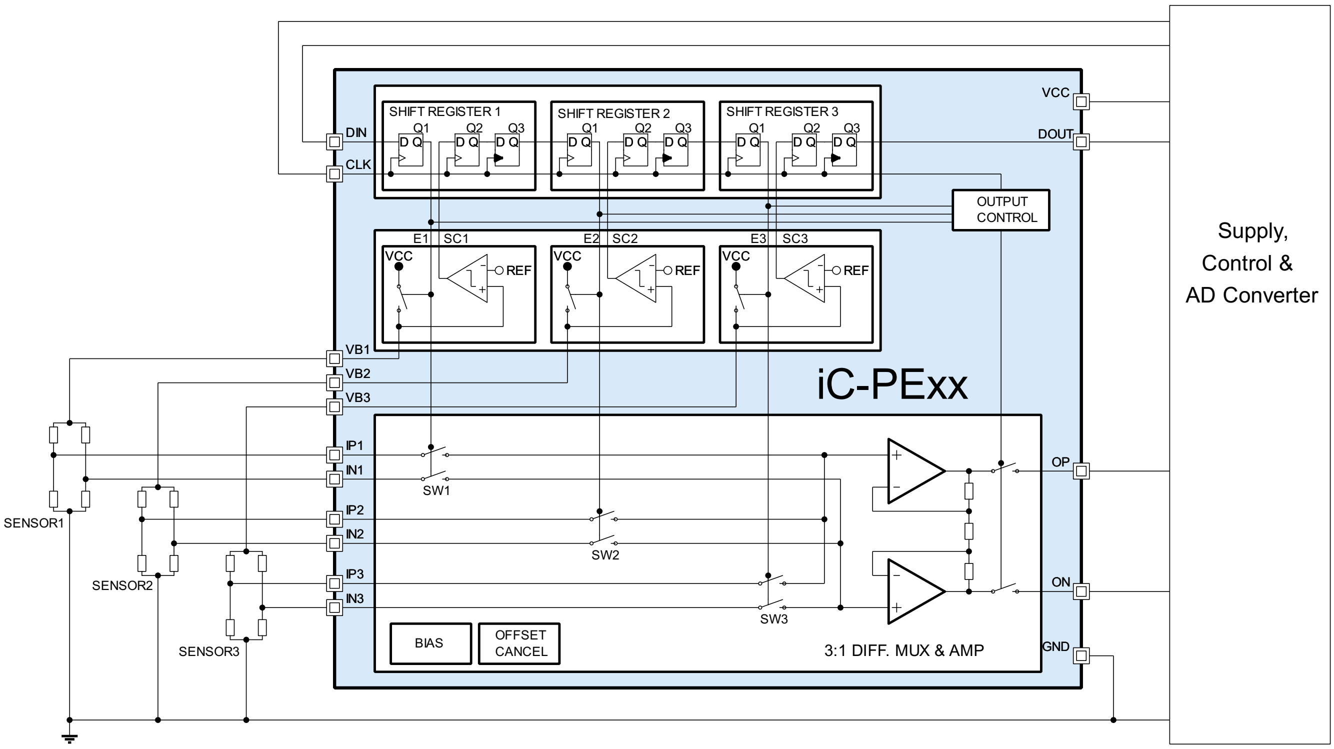


Figure 3: Single chip configuration for sequential reading of 3 bridge type sensors

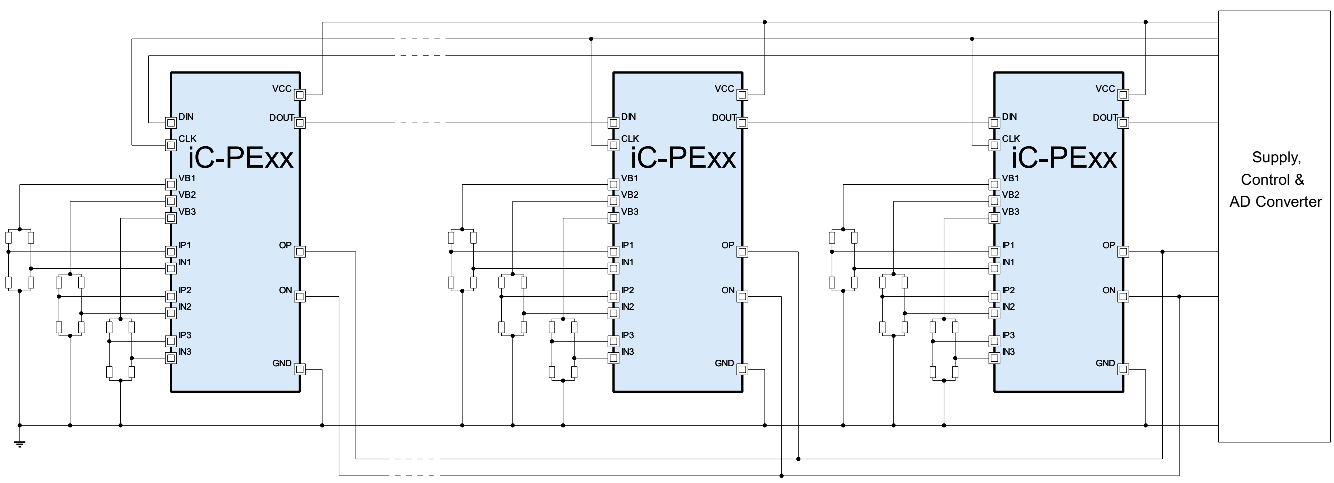


Figure 4: Chain configuration for sequential reading of multiple sensors

PRECISION APPLICATIONS

iC-PExx features low noise and internal offset canceling functions to provide precise signal conditioning. Even extended precision can be achieved if required, by external offset canceling or adding a gain stage. For the external offset canceling option, one of the channels is connected as a voltage reference. This allows measuring the offset of the iC-PExx. This offset can be measured with a precision AD converter and substracted afterwards from the different sensor readings. In case of very weak signals where a higher gain is required, iC-PExx can be configured as an instrumentation amplifier by adding an external precision operational amplifier, iC-HQ for instance.

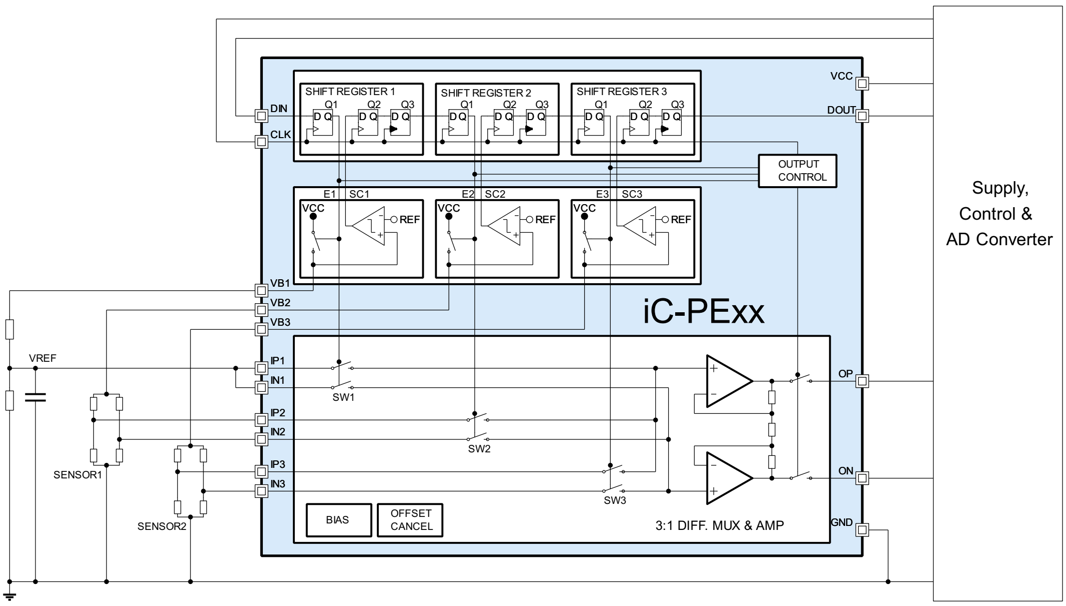


Figure 5: External offset compensation scheme

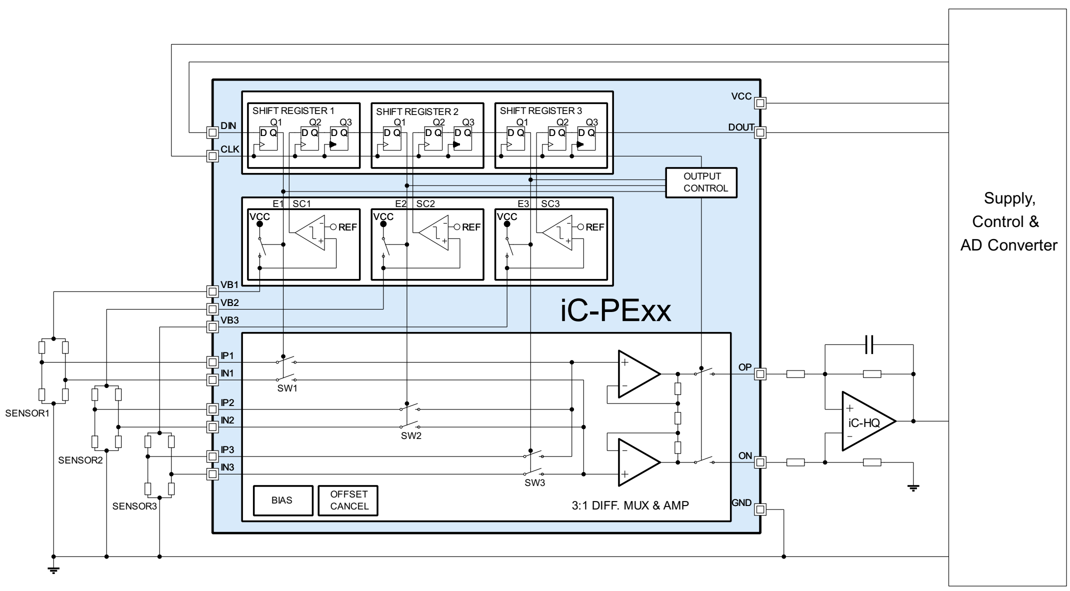


Figure 6: Instrumentation amplifier configuration with external op-amp

SAFETY APPLICATIONS

The iC-PExx is specifically designed for safety applications. In addition to short-circuit protected outputs (sensor supply VB1-3, and signal outputs OP, ON), iC-PExx detects both open-circuit and short-circuit conditions of the sensor supply outputs VB1 to VB3.

An open-circuit is indicated when both analog outputs OP, ON stay high (close to VCC) during reading. Even when an open-circuit is detected, the sequential reading process is not stopped.

A short-circuit is indicated when both outputs OP, ON stay low (close to GND) during reading. When a short-circuit is detected, an internal signal (SC1-3) is generated, stopping the sequential reading process.

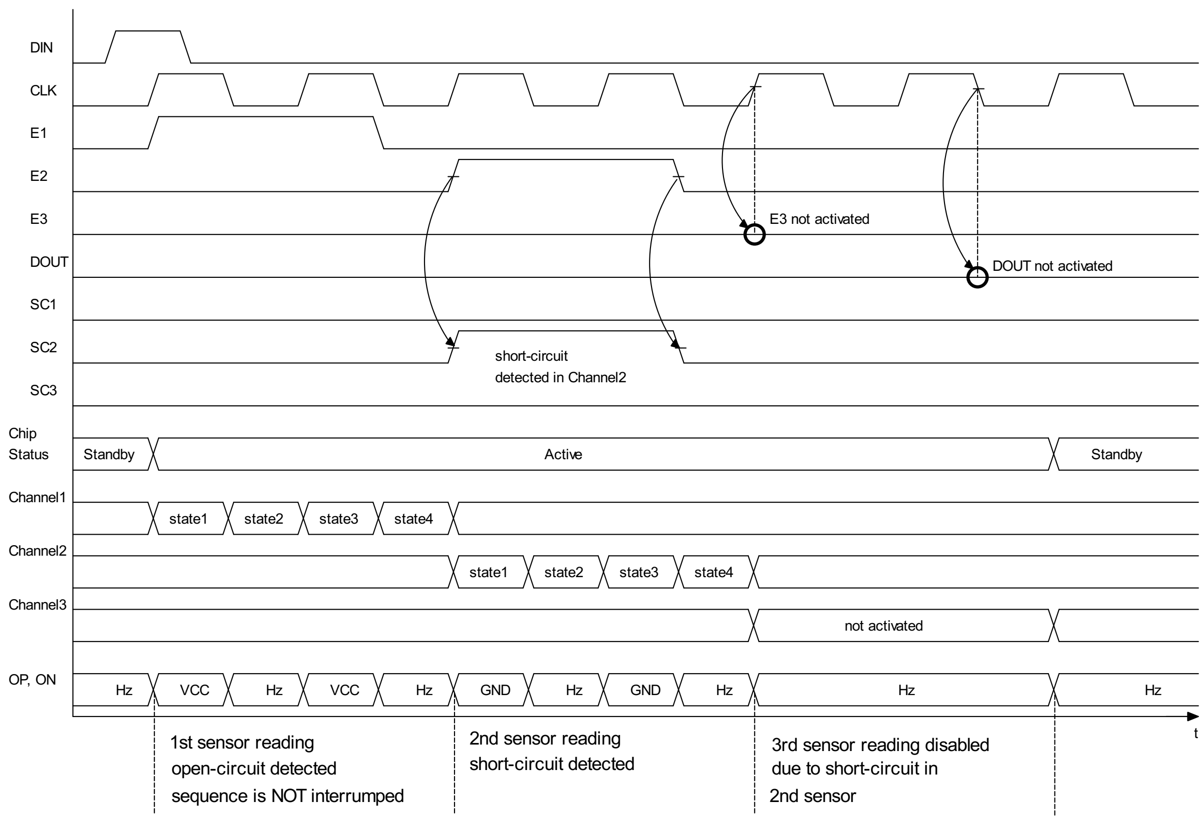


Figure 7: Example of open-circuit and short-circuit detection

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2017-04-05	All	Initial release	all

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PExx	16-pin QFN, 3 mm x 3 mm x 0.9 mm, RoHS compliant	xx = device version	iC-PExx QFN16-3x3
		01: GAIN 1	iC-PE01 QFN16-3x3
		10: GAIN 10*	iC-PE10 QFN16-3x3
		20: GAIN 20*	iC-PE20 QFN16-3x3
		30: GAIN 30	iC-PE30 QFN16-3x3
		50: GAIN 50*	iC-PE50 QFN16-3x3

*) Please contact iC-Haus for availability.

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
E-Mail: dispo@ichaus.com

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (0) 61 35 - 92 92 - 0
Fax: +49 (0) 61 35 - 92 92 - 192
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