

# iC149

## PROGRAMMABLE ns-PULSE GENERATOR

preliminary



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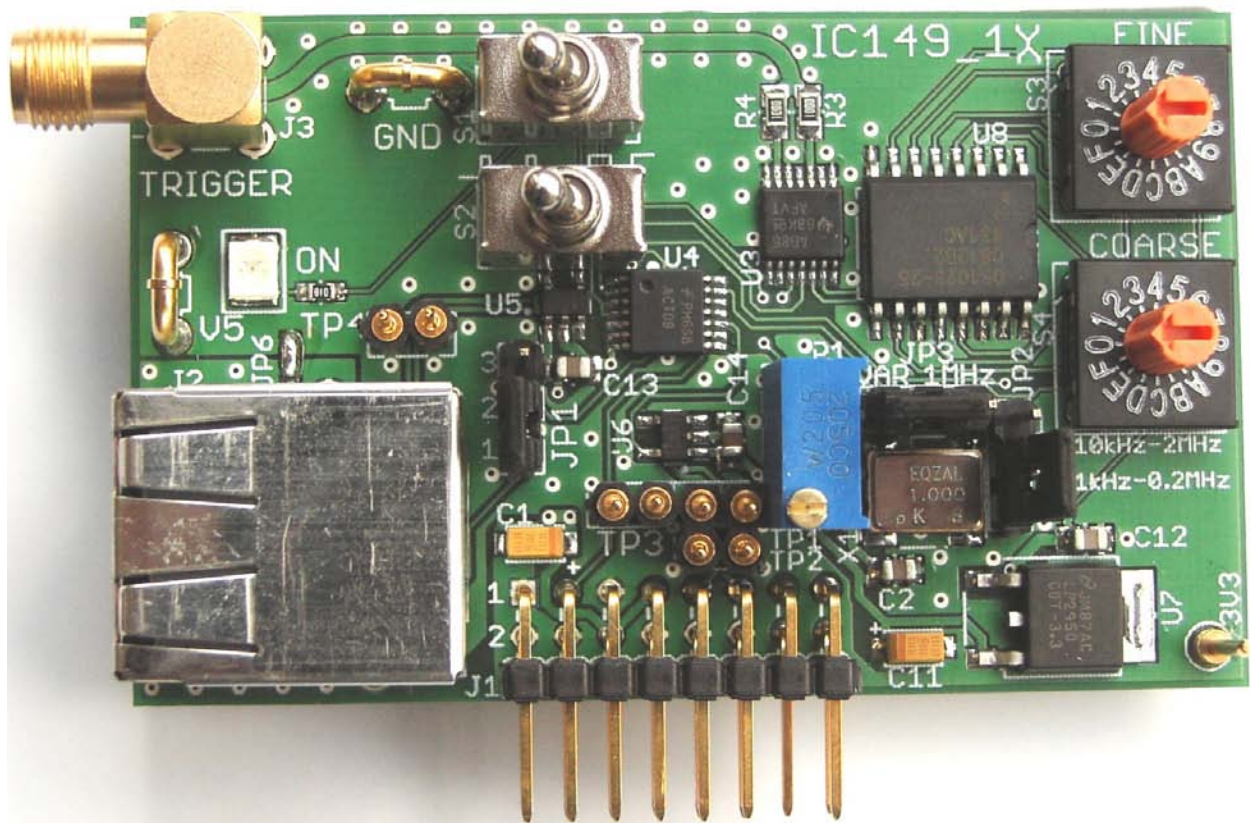
### FEATURES

Pulse width 1 to 64 ns in steps of 0.25 ns  
Fixed crystal stabilised frequency of 1 MHz  
Variable frequency of 1 kHz to 2 MHz  
LVDS und TTL outputs  
Compatible with HG1D, NZN1D, NZP1D

### APPLICATIONS

Pulse generator for fast laser diode drivers

### BOARD



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### DESCRIPTION

Pulse generator iC149 produces pulses with a small duty cycle in the range of ca. 1 ns up to 64 ns max. in steps of 0.25 ns at a pulse frequency of 1 MHz. The pulse width is set by means of two hexadecimal coding switches in coarse and fine steps.

Alternatively a tunable (P1) oscillator can be used.

The pulses are output both as LVDS and TTL signals.

This module can easily be used with the evaluation boards HG1D, NZN1D and NZP1D.

### ELECTRICAL CHARACTERISTICS

Test Conditions:  $T_a = 25\text{ }^\circ\text{C}$

| Item No.            | Symbol            | Parameter         | Conditions   | Min. | Typ.     | Max. | Unit     |
|---------------------|-------------------|-------------------|--|------|----------|------|----------|
| <b>Power Supply</b> |                   |                   |  |      |          |      |          |
| 101                 | V5                | Power Supply      |  | 4.5  | 5        | 5.5  | V        |
| 102                 | I(V5)             | Supply Current    | V5 = 5 V, S1 = ON/OFF, TRIGGER open<br>V5 = 5 V, S1 = ON, TRIGGER 50 $\Omega$ vs. Ground |      | 50<br>75 |      | mA<br>mA |
| <b>Pulse Width</b>  |                   |                   |  |      |          |      |          |
| 201                 | T <sub>pmax</sub> | Maximum Pulsweite | V5 = 5 V, $T_a = 27\text{ }^\circ\text{C}$ , <i>coarse</i> = "F", <i>fine</i> = "F"      |      | 63.75    |      | ns       |
| 202                 | T <sub>pmin</sub> | Minimum Pulsweite | V5 = 5 V, $T_a = 27\text{ }^\circ\text{C}$ , <i>coarse</i> = "0", <i>fine</i> = "C"      |      | 1        |      | ns       |

### PIN CONFIGURATION

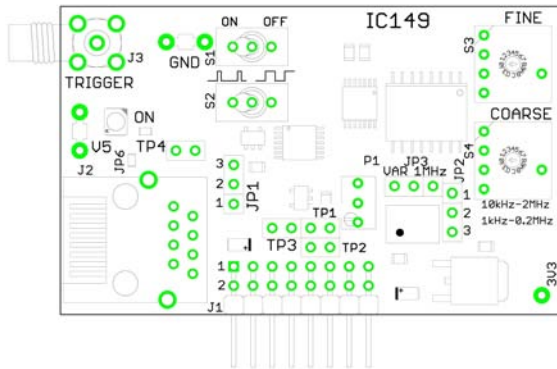


Figure 1: The populated PCB

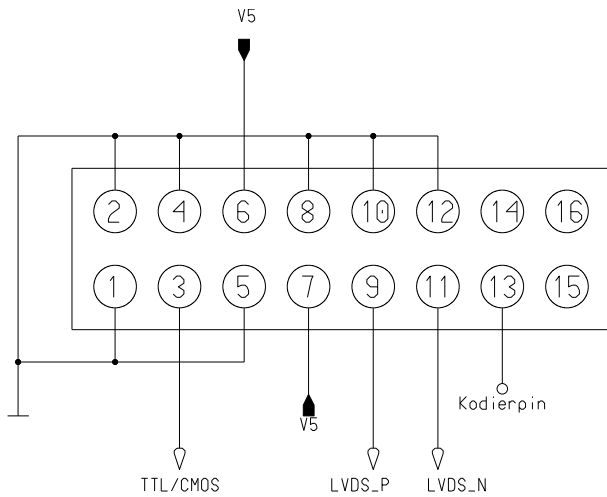


Figure 2: Pin configuration J1

- J1 16 pole pin header for power supply and signal outputs
- J2 RJ45 connector for output signals with LVDS or TTL/CMOS levels
- J3 TRIGGER: SMA connector for trigger output,  $R_{out} = 50 \Omega$
- JP1 Jumper at position 1-2 selects TTL/CMOS signals for J2
- JP2 Jumper at position 1-2: variable frequency from 10 kHz to 2 MHz  
Jumper at position 2-3: variable frequency from 1 to 100 kHz
- JP3 Jumper at position 1-2: crystal stabilised fixed frequency of 1 MHz  
Jumper at position 2-3: variable frequency from 1 kHz to 2 MHz (see JP2)
- S1 Oscillator ON/OFF
- S2 Selector switch: programmable pulse or symmetrical 1 MHz signal
- S3 Coding switch *fine*
- S4 Coding switch *coarse*
- TP1 LVDS signal at J1 (must be terminated with  $100 \Omega$  for measurement purpose)
- TP2 LVDS signal at J1
- TP3 TTL/CMOS signal at J1
- TP4 LVDS signal at J2
- P1 Trimmer for setting the variable frequency
- GND GND
- V5 5 V Power supply
- 3V3 3.3 V

Table 2: Connectors on the PCB

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### BLOCK DIAGRAM

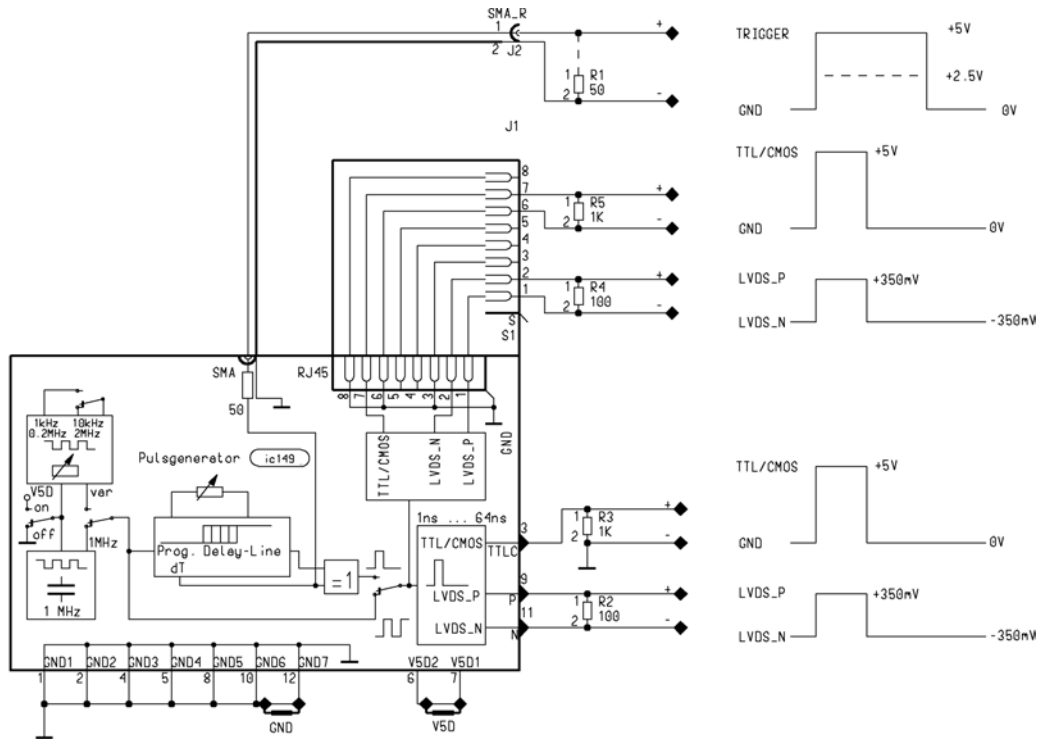


Figure 3: Block diagram of the iC149

### VARIABLE OSCILLATOR

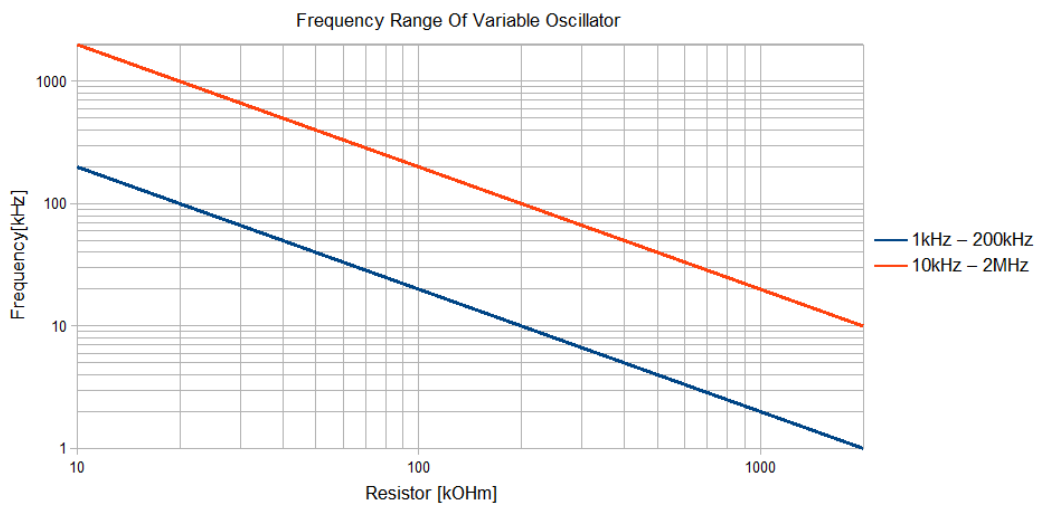


Figure 4: Variable frequency vs. potentiometer setting

### SETTING THE PULSE WIDTH

$$\Delta T = (m * 4 \text{ ns} + n * 0.25 \text{ ns}) \pm 2 \text{ ns}$$

$1 \leq m \text{ (coarse)} \leq 15,$   
 $0 \leq n \text{ (fine)} \leq 15$

$$\Delta T = (m * 4 \text{ ns} + 3.75 \text{ ns}) \pm 2 \text{ ns}$$

$1 \leq m \text{ (coarse)} \leq 15,$   
 $n \text{ (fine)} = 15$

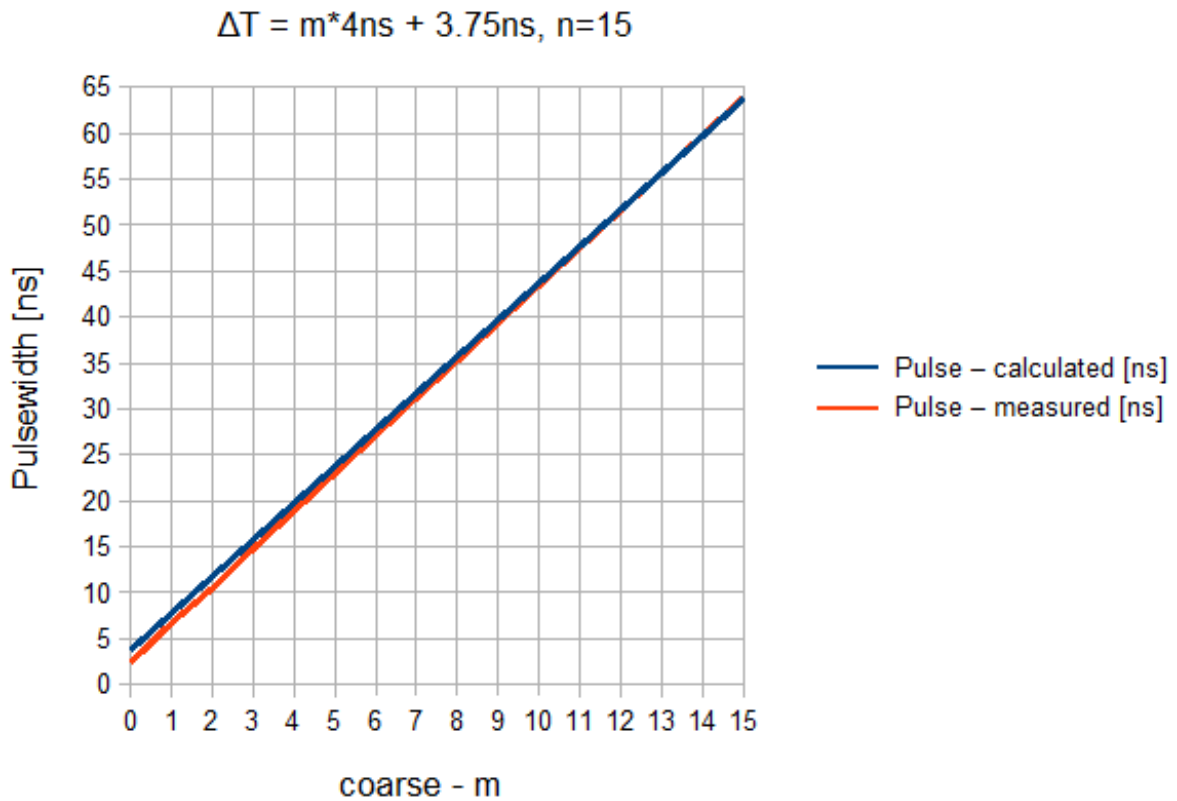


Figure 5: Setting the pulse width "coarse"

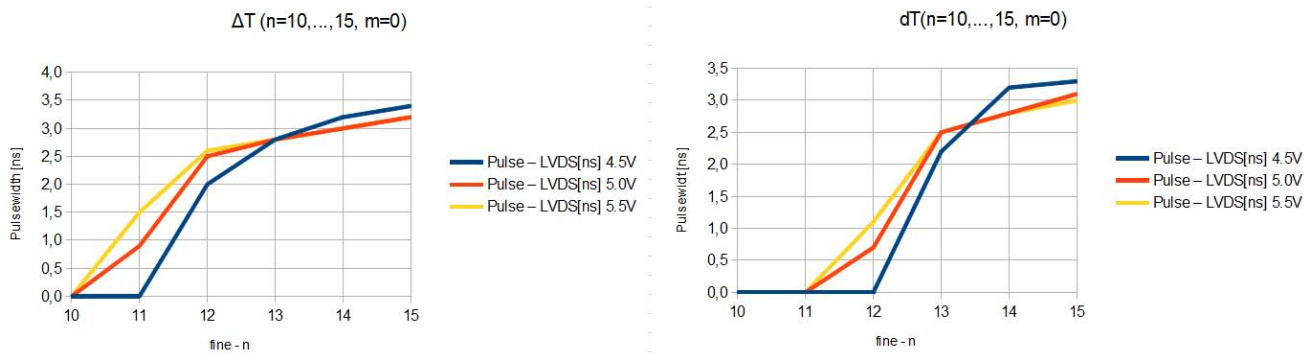


Figure 6: Setting the pulse width "fine", with respect to the supply voltage and device parameter variation

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### SAMPLE PULSES

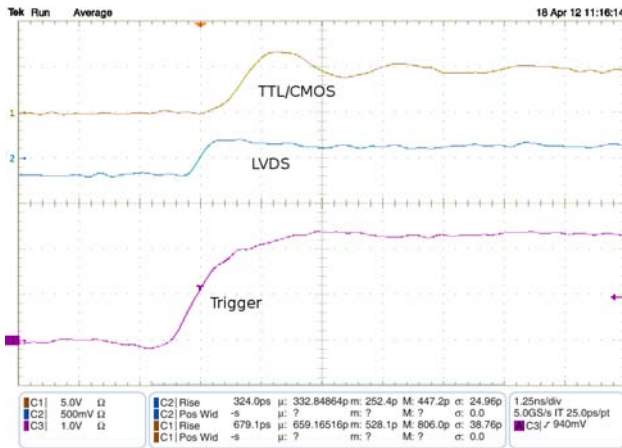


Figure 7: In pulse mode (S2 left hand position) the rising edge of the trigger signal and the LVDS appear simultaneously. The TTL/CMOS has an approx. 1 ns delay.

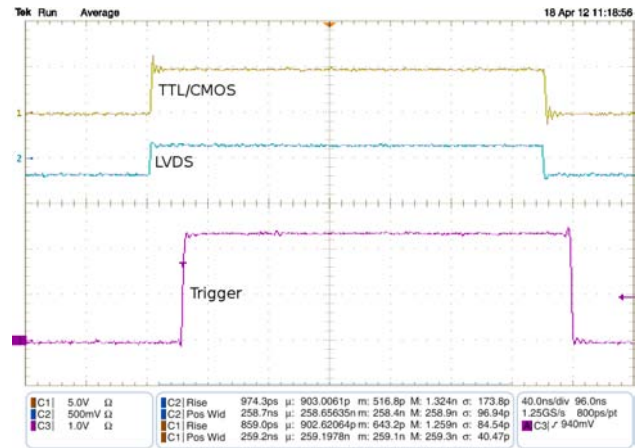


Figure 8: In the symmetrical mode (S2 right hand position) the rising edge of the trigger signal has an approx. 20 ns delay with reference to the output signals.

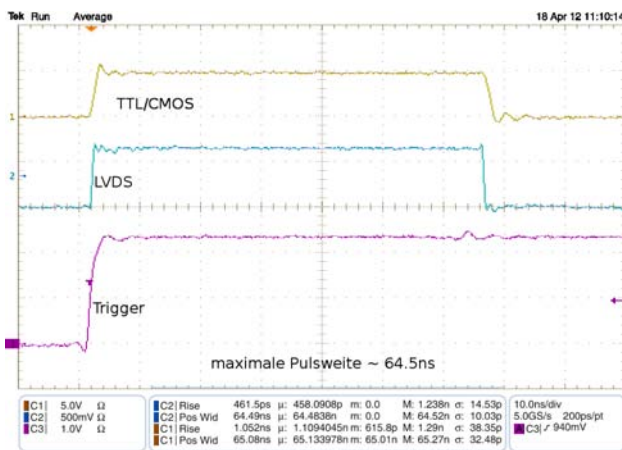


Figure 9: Maximum pulse width at switch setting "FF"

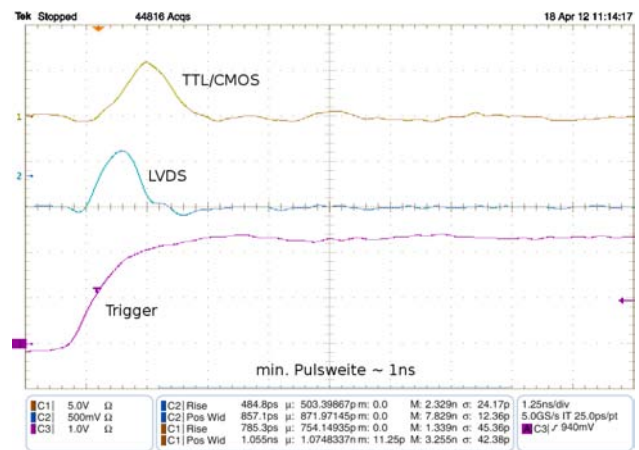


Figure 10: Minimum pulse width at switch setting "0B"



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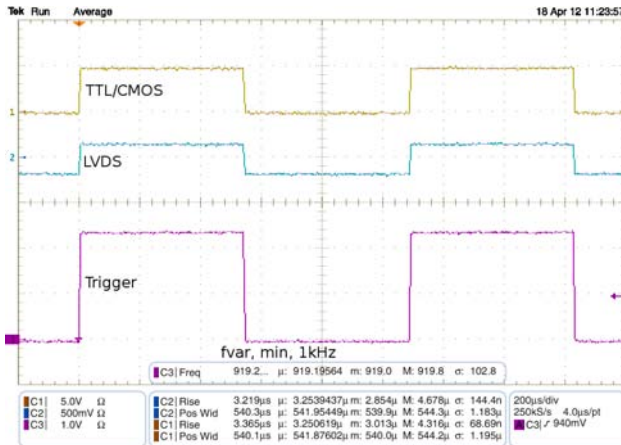


Figure 11: Minimum variable frequency, JP3 = 2-3, JP2 = 2-3, P1 = CCW

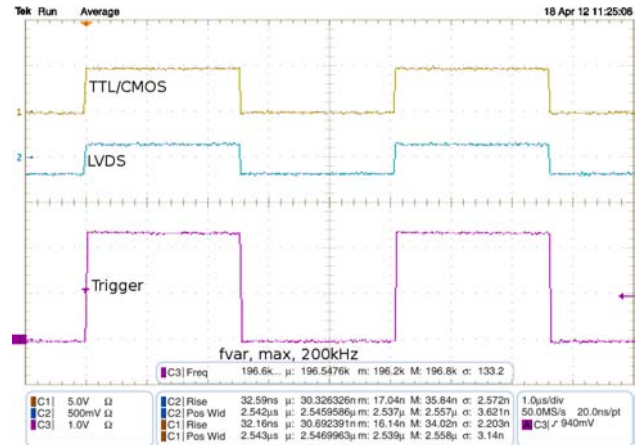


Figure 12: Maximum variable frequency, JP3 = 2-3, JP2 = 2-3, P1 = CW

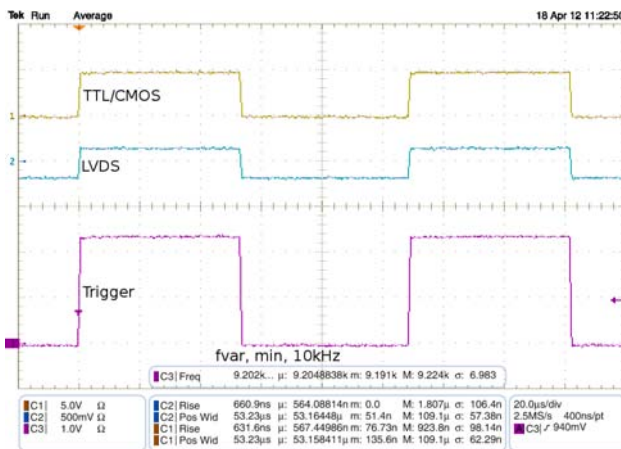


Figure 13: Minimum variable frequency, JP3 = 2-3, JP2 = 1-2, P1 = CCW

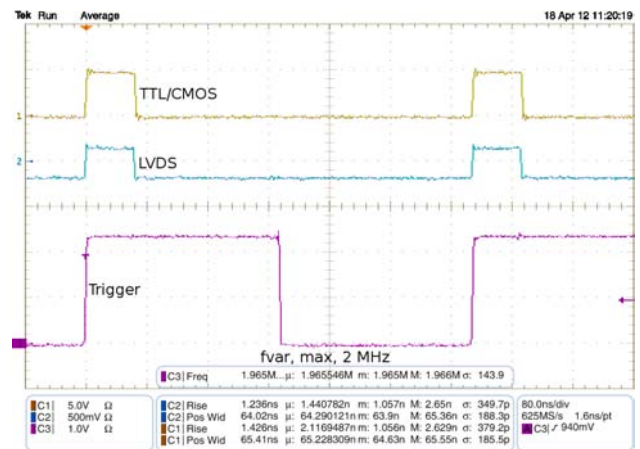


Figure 14: Maximum variable frequency, JP3 = 2-3, JP2 = 1-2, P1 = CW

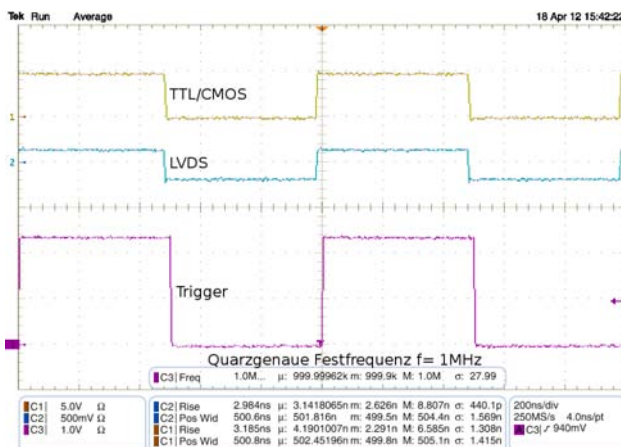


Figure 15: Fixed frequency 1 MHz, JP3 = 1-2

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